P855M CU

Service Manual
P831 Magnetic Tape
Control Unit

The information contained in this manual is based on the documentation available at the time of printing, January 1974. However, should any errors or omissions be discovered, or should any user wish to make any suggestions for improving this manual, he is invited to send his comments to:

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A publication of
PHILIPS-ELECTROLOGICA B.V.
Main Marketing Group - OEM
Apeldoorn, The Netherlands

Pub. No. 5122 991 12471

January 1974

Printed in the Netherlands.

Effective Pages — January 1974

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P831 MAGNETIC TAPE CONTROL UNIT

PRELIMINARY

2.1 INTRODUCTION

The P831 Magnetic Tape Control Unit provides a control interface between a P855M central processor and a Peripheral Equipment Corporation (PEC) model F849/7 magnetic tape formatter. The formatter in turn provides a control interface with up to four PEC model 68X0-9 or 78X0-9 magnetic tape transports. The control unit is connected to the central processor via the standard I/O bus for operation on the multiplex Channel. A block diagram of a typical magnetic tape system is shown in figure 2-1.

2.2 Description

The PEC tape transports (devices) used with the control unit and formatter use the NRZ1 recording technique. The units can operate at 25 ips and 45 ips, with 7 or 9 tracks and a packing density of 200 to 800 bpi. Nine track units have dual stack heads which allow read-after-write working. Additional information is given in the manufacturer's manual.

2.3 Physical Characteristics

The magnetic tape control unit comprises two printed circuit cards mounted together with the power supply modules and the I/O Extender card in a standard 5-card rack, refer to para 2.71 for detailed physical description, including all interconnections.

2.4 Reference Data

General information about the P855M input/output facilities is given in Section I of this manual. This control unit description is based on the following document :

Boolean Book 059 CADOLI 14473.58, run 3351, date 721208

2.5 Tape Formatter

Under control of the P831 Magnetic Tape Control Unit, the formatter selects and controls any one of the connected devices. During a write operation the formatter generates Longitudinal Redundancy (1RC) characters, Cyclic Redundancy Check (CRC) characters (not used with 7-track format) and Vertical Redundancy Check (VRC) bits. These characters and parity bits are used by the formatter during read operations and, during write operations where the device is fitted with dual stack heads for read-after-write working, to check the validity of the data read from tape.

2.6 The CRC character is used for the detection and correction of single track errors within a data block (track format is shown on Figure 2-2). The LRC character gives the longitudinal parity of each data block and is written as the last character in each block. The VRC bit in each character (including check characters) gives odd parity to each character and is written in track four. A gap of four characters separates the last data character of a block from the CRC character and a similar gap separates the check characters.

2.7 File Mark. On command from the control unit the formatter generates a file mark character preceded by a tape gap of approximately 9cm. The file mark character is followed by an LRC character and an interblock gap of approximately 1.5cm. During a read operation the file mark is recognised by the formatter and is signalled to the control unit.

2.8 Gap Generation. The formatter generates the following tape gaps :

- Initial gap of approximately 9cm between the trailing edge of the Beginning Of Tape (BOT) marker and the first data character.
- Inter-block gap of approximately 1.5cm between blocks of data.

2.9 FUNCTIONAL DESCRIPTION

The following description refers to drawings and timing diagrams included with the general text and to the logic diagrams at the end of the section. A block diagram of the control unit is given and is described in the following paragraphs.

Basic I/O bus information and information common to the P855M/P860M range a high speed control units is included in Section I.

2.10 SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

The block diagram (Figure 2-3) shows the major components of the control unit along with data paths and control signals. All data and control lines interfacing with the central processor and with the magnetic tape formatter are shown. (these are described briefly in Table 2-1.) A brief description of each block is given in paragraphs 2-11 through 2-25.

2.11 Address Logic. Decodes the control unit address received on lines BAD02N to BAD05N (see para 2.26).

2.12 I/O Command Logic. Decodes the I/O command received on lines BOF00N to BOF02N (see para 2.29); the control unit goes to the required operational state and the start logic is initiated.

2.13 CU State Logic. Switches to and from specified operational states (see para 2.36) that control the execution of a command.

2.14 Start and Control Logic. Initiated by the I/O command logic this generates CLK2N pulse which enables the Tape Command Decoder and starts the operation in the formatter.

2.15 Halt And Interrupt Logic. Generates Break Requests during data transfers and Program Interrupts to request status exchanges; halts the control unit sequences at the end of an operation or if a serious error occurs.

2.16 Clock Logic. This is a special circuit that generates the CP and CPN timing pulses for use in the control unit.

2.17 Buffer Gating Control. Controls data input to the Buffer Register. Tape instruction information is clocked into the register by ACCION; write data from

Table 2-1. Interface Signals

Signal	Meaning
CPU Interface	
BAD00N to BAD01N	Device address lines
BAD02N to BAD05N	Control unit address lines
DAVN	Device address validation
B0F00N to B0F02N	I/0 command function lines
MCN	Master Clear
E0RN	End of Range signal
AREN	Address recognized
ACCN	Command accepted
B0U00 to B0U07	Not used
B0U08 to B0U15	Data out and tape instruction lines from CPU
BIN00N	Not used
BIN01N to BIN15N	Data in and status lines to CPU
BRN	Break request line
IRN	Interrupt request line
CU to Formatter	
ITAD0 to ITAD1	Tape transport address lines
IGO	Initiate command specified on command lines
IREV	Forward or reverse tape motion indicator
IWRT	Read or write mode indicator
IWFM	Write File Mark
IERASE	Erase tape
IREW	Rewind
I0FL	Off line indicator
ILWD	Last word indicator
IFEN	Formatter enable
IW0 to IW7	Write data lines
Formatter to CU	
IFBY	Formatter Busy indication
IDBY	Data busy indication
ICCG	Check character indication
IHER	Hard Error; read error detected by Formatter
IFMK	File Mark detected
IRDY	Transport ready
I0NL	On line indication
IFPT	Tape transport File Protected
ILDP	Tape transport at load Point
IE0T	End of Tape indication
IWSTR	Write data strobe
IRSTR	Read data strobe
IRP, IR0 to IR7	Read parity line and read data lines

BOU15 is clocked into the register by ACOTR and CWRTF;read data from R0 to R7 is clocked into the register by ACSTRN.

2.18 Buffer Register. This 8-bit register is the main data buffer in the control unit. The input data paths are controlled by READPLSN and data is gated into the register as explained in para 2.16. The output is to the Tape Command Decoder, to BIN15 or to IW0 to IW7 lines.

2.19 BIN Gates. Four quad 2-input multiplexers which load status information (enabled by WST) or read data (enabled by BINEN) on to the BIN lines (via gates controlled by DAV).

2.20 Tape Command Decoder. Decodes tape instructions and sends an appropriate signal to the formatter.

2.21 Read and Write Strobe Logic. Enabled by the Tape Command Decoder and the read or write strobe pulses from the formatter. Produces strobe pulse to synchronize data transfers and to enable Break Request generation.

2.22 Error, File Mark, and Check Logic. Detects data errors signalled by the formatter and control unit errors (para 2.67) which stop the current operation.

2.23 Device Number Logic. Memorizes the device number received on BAD00N and BAD0IN. Used during scanning (para 2.41).

2.24 Device Scanning Logic. Scans connected devices when the control unit is inactive (para 2.41).

2.25 Device State Control. Monitors device (On line and Ready) and Power supply (PWFALN) for operability. When the selected device is operable the Formatter Enable (IFEN) signal is sent to the formatter.

2.26 Addressing

The CU address and the device number are specified on the BAD00N to BAD05N lines which are activated whenever a command is received by the CU. BAD00N and BADOIN specify the device number and are set into the MTADF flip-flops (Figure 2-21, sheet 3) at the start of every command.

BAD02N to BAD05N contain the CU address and must be decoded by the CU. They are compared with the hard-wired CU address preset at system installation time by means of four jumpers on circuit card B (Figure 2-2, sheet 1). A correct CU address on the BAD lines generates the AKDN signal to enable the command decoder (COMMANDS).

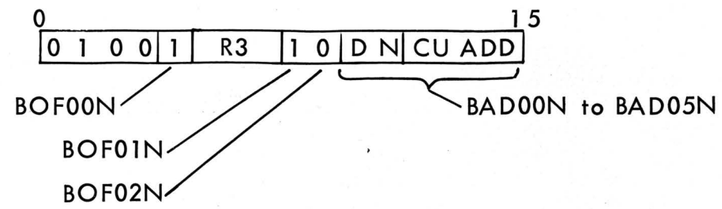
2.27 After the address lines are activated, the Device Address Validation (DAVN) line is activated. DAV and AKD generate the Address Recognized (AREN) signal which is returned to the CPU. DAV also acts as a gating signal for the decoded I/O commands and gates data and status information onto the BIN lines.

2.28 I/O Command

The CU recognizes and responds to the six types of P855M I/O commands described in the following paragraphs. These commands are transferred to the control unit on the BOF00N to BOF02N lines and are always accompanied by the address information (para 2.26). The TST, SST and CIO commands are transferred from the CPU on the Programmed Channel. The INR and OTR commands are transferred on the Multiplex Channel.

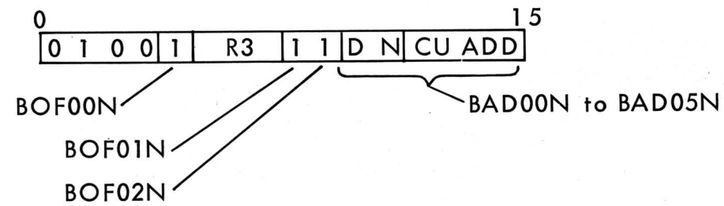
2.29 Command Accept. When a I/O command is received, the BOF lines are decoded if the address is correct (para 2.26). The output from COMMANDS (Figure 2.21, sheet 1) produces the Command Accept (ACCN) signal, via the appropriate gates, which is returned to the CPU. The TST and C1O HALT commands are accepted by the CU at any time. The SST, INR, 0TR and C1O START commands are accepted only if the CU is in the appropriate operational state (see Figure 2-4 and refer to para 2.36).

2.30 Test Status (TST).



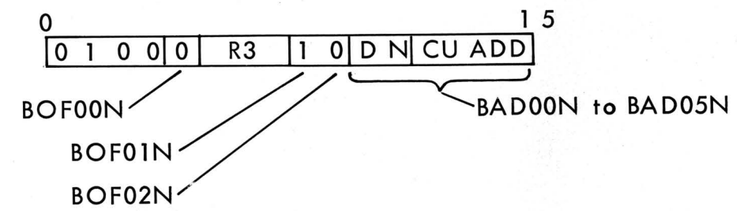
This command is used by the CPU to test the status of the CU before starting an operation or during an operation and is accepted in any operational state. If the CU is in the Inactive State (para 2.37) it responds by sending all zeros to the CPU via the BIN lines. If the CU is in any other state (busy) it responds by sending a 1 bit on BIN line 15; all other BIN lines are not significant.

2.31 Send Status (SST).



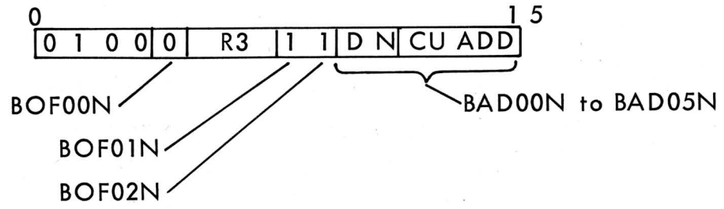
This command is used to transfer the status word from the CU to the CPU on the BIN lines. It is received in response to a program interrupt request (IRN) given when the CU is in the Wait Status state (para 2.40). The bits comprising the status word are listed in Table 2.2. The meaning of each bit, the status flip-flop concerned (in brackets under the meaning) and a brief description of possible reasons for a bit being set are also given.

2.32 C1O STOP Command.



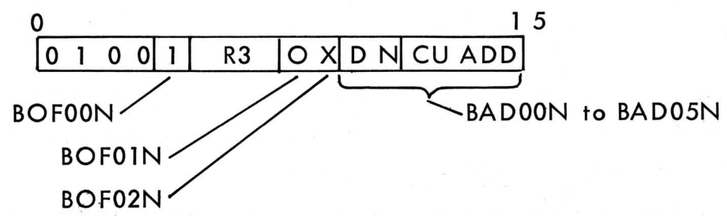
Used under abnormal conditions to halt sequences being performed by the magnetic tape system, the C1O STOP Command is accepted in any operational state. If the formatter has not been initiated (IFBY signal not present) the CU goes to the Wait Status state, requests an SST command from the CPU and then responds with the status word. If the formatter is busy (IFBY signal present) the Formatter Enable (IFEN) signal from the CU is dropped which causes the addressed device to stop at the next interblock gap. During a Write operation (para 2.57) the check characters are written on tape before the device is stopped. The C1O STOP Command does not affect Rewind or Off Line operations.

2.33 C1O START command.



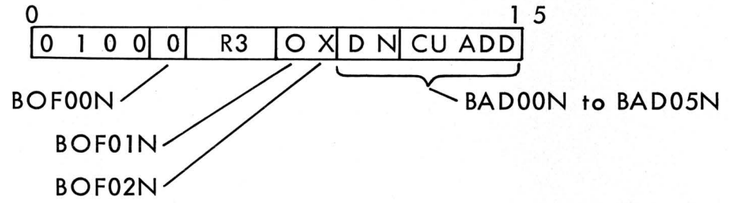
The C1O START command code on the BOF lines is always accompanied by a magnetic tape instruction on the BOU lines (see paragraph 2.43) and Table 2-3). If the CU is in the Inactive state and the address is correct the command is accepted, the CU switches to execute, and the operation definied by the magnetic tape instruction commences. If the command is assigned to an inoperable device (e.g. no File Protect Ring, formatter or transport Busy) it is accepted but not performed if the CU is in the Inactive state. The CU switches to the Wait Status state, sends IRN and waits for the SST command from the CPU. The subsequent status word defines the not-operable condition and gives tape transport number.

2.34 Input Transfer (INR).



This command is received from the Multiplex Channel in response to a Break Request (BRN) from the CU. It is accepted when the CU is in the Exchange state (para 2.39) and is used during read operations (para 2.62) to transfer an 8-bit character from the CU to the CPU on the BIN lines. If it is received during a write operation a Program Error occurs (see Table 2-2).

2.35 Output Transfer (OTR).



This command is received from the Multiplex Channel in response to a Break Request (BRN) from the CU. It is accepted when the CU is in the Exchange state (para 2.39) and is used during write operations (para 2.57) to transfer an 8-bit character from the CPU to the CU on the BOU lines. If it is received during a read operation a Program Error occurs (see Table 2-2).

2.36 Operational States

The P831 control unit uses the four operational states common to all P855M control units. The operational states are set by the two flip-flop sequensor F0-F1 (see Figure 2-4) which is controlled by the command codes received from the CPU and by the operation being performed by the CU. Figure 2-4 shows the relationship between the states and the various command and control signals; the two-bit F-code is shown on each block. The logic is shown on Figure 2-21, sheet 1.

2.37 Inactive (F0 - F1 = 0 - 0). In this state the control unit is in standby mode waiting for a CIO START command and scans the connected tape transports via the formatter to test for operability. Ths control unit is switched to the Wait Status state when a device becomes ready (IRDY signal from formatter) at the end of a rewind operation or when a transport comes on line IONL signal from formatter).

Table 2-2. P831 Magnetic Tape CU Status Word

BIN BIT	MEANING	DESCRIPTION
15	Device Not Operable (Formatter or addressed tape unit.) (NOOPF)	Indicates possible operator intervention required. Set for one of the following reasons : interlocks in Formatter not made; initial load not complete; tape transport is off line; power off on Formatter.
14	Throughput Error (THRF)	Set during a read/write operation if the multiplex channel does not reply to Break Request within the required time. Data exchange is stopped.
13	Data Fault (DTF)	Set when a vertical or longitudinal parity error occurs during read, write or search operations; and when a CRC error is detected during read forward operations.
12	Incorrect Lenght (ILF)	Set during a read command when the tape block length differs from the channel block length
11	Program Error (PREF)	Set for one of the following reasons : an OTR command received during a read operation or an INR command received during a write operation; when a Write Edit command is not preceded by a Backward Space Block Edit command; when a C1O is accompanied by an invalid code on the B0U lines.
10	End of tape (EOT) (EOTF)	Indicates that the EOT marker on the tape has been sensed during forward (read, write, search, space block) operations.
9 8	Tape unit number (TADF0; TADF1)	Give number of tape transport for which the status word is given to the CPU.
7	Not used	
6	File Protect. (No Write enable Ring mounted on tape reel.) (FPTW)	Set when the CU receives a write, write file mark, erase command when the selected tape unit is file protected. Any data exchange is stopped.
5	Load Point (BOT) (LDPT)	Indicates the beginning of tape (BOT). Set when the selected tape unit is at the Load Point.
4	Not used	
3	File Mark (FMKF)	Indicates that a File Mark has been sensed or a File Mark format has been detected with a data fault during a read, space block or search operation.
2	Rewind (TRWD)	Indicates that the selected tape unit is in the rewind condition.
1	Was Not Ready (TWNRF)	Indicates that a device has entered the ready condition following an inoperable status or a tape rewind condition.

Table 2-3. CIO Start Commands (Magnetic Tape Instructions)

CODE (BOU) 10 11 12 13 14 15	NAME	DESCRIPTION
1XX0XX	Off Line	The selected device is put into the off line condition and becomes inoperable
1XX1XX	Rewind	On the selected device, the tape is rewound at high speed to the Load Point
000011	Write	The CU and selected device are prepared for recording data on tape. Data is transferred from the CPU using OTR commands.
010001	Write File Mark	A File Mark block is written on tape. (A unique coded character, 0001001102, followed by an LRC.)
011001	Erase Gap	The tape is advanced approximately 9cm while erasing. This command is normally given to erase a portion of tape that cannot reliably record data.
000010	Read Forward	This command initiates a read data from tape operation. Data is transferred from the CU to the CPU using INR commands.
010000	Search File Mark forward	The tape is moved forward to the interblock gap beyond the next File Mark on tape.
010100	Search File Mark backward	The tape is moved backward to the interblock gap beyond the next File Mark, or to the Load Point.
000000	Forward Space Block	The tape is moved one block forward to next interblock gap.
000100	Backward Space Block	The tape is moved one block backward to the next interblock gap.

The control unit is switched to the Inactive state from Wait Status on the trailing edge of an SST command, or from Execute after the execu cution of an Off line or Rewind instruction.

2.38 Execute (F0 - F1 = 0 - 1). This state is used for the exchange of data (in 8-bit characters) and command information between the control unit and the formatter. (During Off Line and Rewind operations control information is also sent to the addressed device.) The control unit switches to the Execute state on the trailing edge of a CIO START command received on the Programmed Channel, or on the trailing edge of an INR/OTR command received from the Multiplex Channel.

2.39 Exchange (F0 - F1 = 1 - 1). The Exchange state is used for the exchange of data (in 8-bit characters) between the control unit and the central processor.

The control unit is switched to this state on the leading edge of a write/read strobe pulse (STR) when a Break Request (BSN) is sent to the central processor. When a character is successfully transferred, the control unit returns to Execute (trailing edge of INR/OTR) to perform the character transfer between it and the formatter. If a block transfer is completed the control unit switches to Wait Status (via FLOSET).

2.40 Wait Status (F0 - F1 = 1 - 0). The CU switches to this state at the end of a correctly executed operation (except Rewind and Off Line) when a fault occurs or when a non-operable tape transport becomes operable. The interrupt request (IRN) is sent to the CPU asking for an SST command. When the SST is received the status word is sent to the CPU on the BIN lines. The CU switches to the Inactive state on the trailing edge of the SST command.

2.41 Scanning

In the inactive state the control unit scans the connected devices. The current device number (set during the last operation) in the Up/Down Counter TADF (see Figure 2-21, sheet 3) is decremented every TADFCL time. The binary number on ITAD0 and ITAD1 is sent to the formatter to test the addressed device. If a change is detected the control unit switches to Wait Status; if no change is detected the next device is tested.

2.42 The control unit scan timing for a device becoming ready is shown on Figure 2-5; the logic is shown on Figure 2-21, sheet 3. Each time TADF is decremented the new number is set into TNRSRWDF and output TNRSN primes flip-flop TWNRF. If the addressed device is ready the IRDY signal received from the formatter sets flip-flop TWNRF. The scanning is stopped via TWNRN0PF which also sets the control unit to Wait Status (via FOZIN). The subsequent status word (see Table 2-2) contains the device number in bits 8 and 9 and bit 1 is set.

2.43 Magnetic Tape Instructions

The magnetic tape instructions are extensions of the CIO START command and are transferred from the CPU on BOU10 to BOU15. When a CIO START command is received the code on the BOU lines is loaded into the BUFFER (see Figure 2-3) The BUFFER contents are decoded, the relevent instruction signals are sent to the formatter along with the IPAR, IDEN, IREV and IGO signals and the control unit is set up for the operation to be performed. Table 2-3 lists the instructions used, gives the BOU line codes and gives a brief description of each instruction; initial timing is shown on Figure 2-6.

2.44 Off line. This instruction is used to put the addressed device off line. Timing is shown on Figure 2-7. When the command is accepted the control unit switches to the Execute state and sends the IOFL signal directly to the addressed device. The IRDY and IONL signals from the formatter are dropped and the control unit returns to the Inactive state on the trailing edge of the CLK2N pulse.

2.45 When a device is off line, operator intervention is required to put it back on line. An instruction addressed to an off-line device results in the control unit going to Wait Status and generating an interrupt request (IRN) to the CPU. The subsequent status word gives the device number and bit 15 is set.

2.46 Rewind. The instruction causes the tape on the addressed device to be rewound at high speed to the Load Point. The timing is the same as that for Off-Line instructions and is shown on Figure 2-7. When the command is accepted the control unit switches to the Execute state ans sends IREW directly to the addressed device. The IRDY signal from the formatter is dropped and the control unit returns to the Inactive state on the trailing edge of the CLK2N pulse.

2.47 The maximum rewind time is 192 seconds (for 2400 feet of tape) and when the Load Point is reached the condition is detected by the control unit during scanning (para 2.41). An instruction addressed to a device executing a rewind operation results in the control unit being switched to Wait Status and sending the program interrupt request (IRN) to the CPU. The subsequent status word gives the device number in bits 8 and 9 and bit 15 is set.

2.48 Erase gap. This instruction is a dummy write operation and is used to erase approximately 9cm of tape on the addressed device. Timing is shown on Figure 2-8. When the command is accepted, the instruction on the BOU lines is read into the Buffer and the IREV and IWRT signals are sent to the formatter. The control unit switches to the Execute state on the trailing edge of the CIO. The instruction is decoded and the IGO and IERASE pulses are sent to the formatter at CLK2N time; the formatter responds with the IFBY signal.

2.49 When the device is up to speed the IDBY signal is received from the formatter and the device erases a portion of tape. At the end of the device operation the formatter drops IDBY, the control unit is switched to Wait Status and sends the program interrupt to the CPU. The Subsequent status word contains the device number in bits 8 and 9; if the end of tape (EOT) area is detected bit 10 is also set.

2.50 Space One Block (Forward/Backward). Space block operations cause the tape on the addressed device to run forward or backward until the next interblock gap is sensed. Timing is shown on Figure 2-9. When the command is accepted the instruction is read into the BUFFER and the direction indication (IREV : high when forward; low when backward) is sent to the formatter. The start logic is initiated and the control unit switches to Execute on the trailing edge of the CIO START. At CLK2N time the IGO pulse is sent to the formatter to initiate the operation; the formatter responds with IFBY.

2.51 When the device is up to speed, IDBY is received from the formatter and the tape is moved in the required direction. The IDBY signal goes inactive when the tape operation is completed; the control unit switches to Wait Status and the program interrupt request (IRN) is sent to the CPU. The subsequent status word contains the device number in bits 8 and 9; bit 3 is set if a file mark is detected; bit 5 is set if the Load Point (BOT marker) is detected; bit 10 is set if the EOT marker is detected.

2.52 Write File Mark. The instruction is used to write a file mark block on tape (one character, 000100102, followed by an LRC character). Timing is shown on Figure 2-10. When the instruction is decoded the Forward (IREV high) and Write (IWRT low) signals are sent to the Formatter. At CLK2N time the IWFM signal is sent along with the IGO pulse. The formatter responds with the IFBY signal and, after an extra long delay (for the file mark gap on tape after the device is up to speed), the IDBY signal is returned.

2.53 When the operation on the device is finished the IDBY signal goes inactive (high). The control unit is switched to Wait Status via SETWST and sends the program interrupt request to the CPU. In the subsequent status word bits 8 and 9 give the device number; bit 13 is set if a parity error is detected by the formatter; bit 10 is set if the operation is performed in the EOT area.

2.54 Search File Mark (Forward/Backward). Search instructions are used for file mark detection on tape. The operation is similar to that for a Read One Block operation (para 2.62) but there is no data exchange; the formatter detects the file mark internally. Timing is shown on Figure 2-11. When the command is accepted, the IWRT and IREV signals to the formatter are forced high (IREV is low for a backward operation) and the control unit goes to Execute. The formatter returns the IFBY signal, in response to the IGO pulse, on the trailing edge of CLK2N.

2.55 When the addressed device is up to speed the formatter sends IDBY to the control unit. The tape runs in the appropriate direction and stops at the interblock gap after the detected file mark. When the file mark is detected the IFMK signal from the formatter sets the FMKF flip-flop. When the IDBY signal goes inactive the control unit switches to Wait Status and sends the interrupt request to the CPU.

2.56 The subsequent status word contains the device number in bits 8 and 9; bit 3 is set (file mark); bit 5 is set if the operation is performed in the BOT area; bit 10 is set if the operation is performed in the EOT area. If the operation is performed on a blank tape, the tape is moved to the EOT (forward) or the BOT (backward). No interrupt request is sent to the CPU and the control unit becomes inoperable.

2.57 Write One Block. The write instruction is used to record a block of data on tape. Figure 2-12 gives the timing for a typical block transfer to a 9-track tape transport with a tape speed of 45ips.

2.58 When the instruction is accepted the IWRT signal is forced low and IREV is forced high, the start logic is initiated and the control unit switches to Execute on the trailing edge of the CIO START command. At CLK2N time STRN (Figure 2-21, sheet 2) is generated to set the break request flip-flop BRF; IGO is generated to initiate the formatter sequence. Formatter Busy (IFBY) is received, the pre-record delay in the formatter begins and the control unit switches to Exchange. When the device is up to speed IDBY is received and the control unit sends a break request (BSN) to the Multiplex Channel.

2.59 The Multiplex Channel sends an OTR command on the BOF lines with the first data character on the BOU lines and the CU switches to the Execute state. Approximately one character time after IDBY is activated, the Formatter sends a Write Strobe (IWSTR) pulse which samples the Write Data lines (IW0 - IW7) and initiates another Break Request.

2.60 The second character is received and the procedure continues, characters being received from the Multiplex channel with OTR commands in response to Break Requests initiated by IWSTR pulses from the formatter. The CU alternates between the Exchange and Execute states to allow the transfer. At the end of the block the EOR signal is received from the channel (with the last data character). The Last Word (ILWD) signal is sent to the Formatter which then causes the CRC character and/or the LRC character to be written on tape. For 7-track transports, only the LRC character is written.

2.61 The post-record delay is started for transports with single-stack heads immediately after the LRC character is written. Transports with dual-stack heads perform a read-after-write data check and then initiate the post-record delay. At the end of this delay, IDBY from the formatter goes inactive (high) and the CU switches to the Wait Status state. If a data error is detected (para 2.68) the Hard Error (IHER) signal from the formatter sets flip-flop DTF.

2.62 Read One Block. The read instruction is used to read a block of data from tape. Figure 2-13 gives the timing for a typical block transfer from a 9-track tape transport with a tape speed of 45ips.

2.63 When the command is accepted the read instruction code on the BOU lines is read into the BUFFER (Figure 2-21, sheet 2). The IWRT and IREV signals to the formatter are forced high and the control unit switches to Execute. At CLK2N time the read data path to the BUFFER is opened (READPLSN). The formatter returns the IFBY signal, in response to the IGO pulse, on the trailing edge of CLK2N.

2.64 When the tape transport is up to speed, Data Busy (IDBY) is received from the formatter. The formatter sends a Read Strobe (IRSTR) pulse with the first data character read from tape, a Break Request is initiated, the character is made available to the BIN register (BINR) and the CU switches to the Exchange state. In response to the Break Request, the Multiplex Channel returns an INR command. The data character is put on the BIN lines, the control unit switches to the Execute state and waits for the next character.

2.65 Subsequent character transfers are effected as outlined . Characters are received from the formatter along with IRSTR pulses which initiate Break Requests and the channel sends INR commands to collect the data. The CU switches between the Execute and Exchange states to allow the transfers.

2.66 After the last data character is read, there is a four character gap and the CRC character is received and transferred to the CPU along with the ICCG signal. (This is the LRC character in 7-track format.) After a further four character gap the LRC character is received and sent to the CPU. The CU receives the EOR signal from the Multiplex Channel to coincide with the arrival of the LRC character. The EOR signal checks for incorrect block length and the CU switches to the Wait Status state.

2.67 Error Detection

All data transfers take place using odd vertical parity and all data error detection functions are performed in the formatter. Any data errors are signalled to the control unit. Error detection in the control unit is confined to program, throughput, incorrect length and not operable errors.

2.68 Data errors. When a data error occurs (VRC bit, CRC and LRC character checks) it is detected by the formatter during read or read-after-write operations. The formatter signals the control unit with the IHER line (Hard Error) which sets Data Fault flip-flop DTF. Data errors do not stop data transfers and when the control unit goes to Wait Status at the end of the operation, bit 13 is set in the subsequent status word.

2.69 Control Unit Error Detection. When the control unit detects one of the following errors the current operation is stopped. The control unit is switched to Wait Status and the appropriate bit is set in the subsequent status word.

- Not Operable : If the selected tape transport goes off-line after the control unit has accepted a CIO START Command flip-flop NOOPF (Figure 2-21, sheet 3) is set. The Formatter Enable (IFEN) signal goes inactive and bit 15 of the status word is set.
- Throughput Error : This error occurs when the Multiplex Channel fails to respond to a break request within the required time. Flip-flop THRF (Figure 2-21, sheet 2) is set and bit 14 of the status word is set.
- Incorrect Length : If the block length on tape differs from data block length in the Multiplex Channel flip-flop ILF (Figure 2-21, sheet 2) is set when the EOR signal is received. Bit 12 of the status word is set.
- Program Error : This error occurs when the Multiplex Channel sends an unrecognizable code on the BOF lines, if an OTR is received during read operations, or if an IRN is received during write operations. Flip-flop PREF (Figure 2-21, sheet 2) is set and bit 11 in the subsequent status word is set.

2.70 CONTROL FLIP-FLOPS

The following table lists and describe the most important flip-flops in the control unit :

Mnemonic	Description
BRF	Breack request flip-flop; set during data transfers by STRN, reset by CECHN when an OTR or an INR command is received.
CCGF1 - CCGF2	Check character detection flip-flops. CCGF1 is set on the trailing edge of IRSTR pulse if ICCG is active; CCGF2 is set on the trailing edge of IRSTR pulse if CCGF1 is set and ICCG is active (indicates incorrect length).
CREADF	Function flip-flop (see COMMEN, Figure 2-21, sheet 2); set when a read tape instruction is decoded.
CSFMKF	Function flip-flop (see COMMEN, Figure 2-21, sheet 2); set when a search file mark instruction is decoded.
CWRTF	Function flip-flop (see COMMEN, Figure 2-21, sheet 2); set when a write tape instruction is decoded.
DTF	Data fault flip-flop; set by IHER line when the formatter detects a data error.
EOTF	End of tape flip-flop; set when the formatter detects the EOT area.
FO-F1	Two flip-flop sequensor (para 2.36).
FMKF	File mark flip-flop; set when a file mark is detected during search file mark or read operations.
FENF	Formatter enable flip-flop; reset at the start of an operation and enables formatter by IFEN line; set by one of the Halt conditions and IFEN goes inactive.

Mnemonic	Description
HALTF1	Stop condition flip-flop, set for one of the following reasons : search file mark instruction attempted in the E0T area; any reverse instruction attempted when tape is at Load Point; any write instructions attempted when the tape is file protected; at the end of a rewind instruction.
HALTF	Stop condition flip-flop; set at the end of a correctly executed instruction.
ILF	Incorrect length flip-flop; set when the tape block length differs from the Multiplex block length.
MTADF0 - MTADF1	Device number flip-flops; memorize the selected device number at the start of a command (ACCI0).
NOOPF	Not operable flip-flop; set when a device becomes not operable (para 2.69).
PREF	Program error flip-flop; (para 2.69).
STAF - STAF1	Part of the start logic. STAF is reset at the beginning of a command to tprime the program interrupt and is set at the end of an operation (by NSST or ACSST). STAF1 generates reset pulse (STWZ0N; RSTWZ 0N) at the start of an operation.
STF, STF1, STF2	Start flip-flops which generate the CLK1 and CLK2N pulses.
STRCF1 - STRCG2	File mark detect flip-flops. Set on the first and second character of any operation. STRCF1 is set on the trailing edge of the first IRSTR pulse and reset on the trailing edge of the third IRSTR pulse. STRCF2 is set on the trailing edge of the second IRSTR pulse and reset at the end of the operation.
TNRF0 - TNRF3	These flip-flops record the selected device number.
TRWD0 - TRWD3	These flip-flops record the number of any device that is executing a rewind operation.
TWNRF	Was not ready flip-flop. Set when a device becomes ready.

2.71 PHYSICAL DESCRIPTION AND INTERCONNECTIONS

The P 831 Magnetic Tape Control Unit comprises two printed circuit cards mounted in a standard 5-card rack along with an I/O Extender card (IORC) and the power supply modules (see Figure 2-15). The I/O Extender card is described in Section 1 and modular power supply information is included as Appendix B.

2.72 Printed Circuit Cards

The control unit logic is contained on standard P 855 logic cards. The cards are called PECA and PECB; their relative mounting positions are shown on Figure 2-15 and card layout on Figures 2-16 and 2-17.

2.73 Interconnections

General cabling and connection information is given on Figure 2-15. I/O cabling information between the 5-card rack and the central processor is given in Section 1. Table 2-4 lists the connections between the IORC card and the control unit cards; Table 2-5 lists the control unit card interconnection; Table 2-6 gives the cable connections between the control unit and the formatter.

Table 2-4. I/O Card Connections

Signal	I/O Pin Nr	PECA Pin Nr	PECB Pin Nr	Signal	I/O Pin Nr	PECA Pin Nr	PECB Pin Nr
BAD00N	2A22	2B22		BOU14	2A05	2B05	
BAD01N	2A24	2B24		BOU15	2A11	2B11	
BAD02N	2A25		2A25	DAVN	2A14		2A14
BAD03N	2A13		2A13	EOR	2A02		2A02
BAD04N	2A15		2A15	MCN	2A12		2A12
BAD05N	2A16		2A16	ACCN	1A13		1A13
BOF00N	2A04		2A04	AREN	1A14		1A14
BOF0IN	2A03		2A03	BIN01N	1A04		1A04
BOF2N	2A01		2A01	BIN02N	1A05		1A05
BOU00	2A28		2A28	BIN03N	1A06		1A06
BOU01	2A27		2A27	BIN04N	1A07		1A07
BOU02	2A26		2A26	BIN05N	1A08		1A08
BOU03	2A23		2A23	BIN06N	1A09		1A09
BOU04	2A21		2A21	BIN07N	1A10		1A10
BOU05	2A20		2A20	BIN08N	1A21		1A21
BOU06	2A19		2A19	BIN09N	1A28		1A28
BOU07	2A18		2A18	BIN10N	1A29		1A29
BOU08	2A17	2B17		BIN11N	1A30		1A30
BOU09	2A08	2B08		BIN12N	1A31		1A31
BOU10	2A09	2B09		BIN13N	1A26		1A26
BOU11	2A10	2B10		BIN14N	1A22		1A22
BOU12	2A07	2B07		BIN15N	1A27		1A27
BOU13	2A06	2B06		BSN	1A16		1A16
				IRN	1A15		1A15

Table 2-5. Control Unit Inter-card Connections

Signal	PECA Pin Nr	PECB Pin Nr	Signal	PECA Pin Nr	PECB Pin Nr
ACINR	1A22	1B22	CSFMKF	2A10	2B10
ACCIO	2A27	2B27	CSHERN	2A11	2B11
ACCION	2A25	2B25	DBYN	1A07	1B07
ACOTR	1A17	1B17	DBY	2A01	2A01
ACSST	2A17	2B17	EOTB	1A18	1B18
CLK2N	2A13	2B13	FBY	1A05	1B05
CCGF1N	2A02	2B02			
DBFBYZ0	2A24	2B24	FMK	1A06	1B06
FENN	2A28	2B28	FPTWN	1A21	1B21
F1G0N	1A03	1B03	HALT1N	2A26	2B26
HALT1	1A20	1B20	HALT2	1A11	1B11
MCLN	2A20	2B20	HERBN	1A13	1B13
NOOPFORN	1A31	1B31	HERB	1A09	1B09
SCANCLKN	1A23	1B23	LDPN	2A22	2B22
STWZ0N	2A05	2B05	NOOP	1A19	1B19
TADFSN	2A23	2B23	PREFZ1N	1A16	1B16
BUF0	1A26	1B26	PRE	1A12	1B12
BUF1	1A27	1B27	REW	1A14	1B14
BUF2N	1A30	1B30	RSTRB	1A04	1B04
BUF2	1A28	1B28	STR	1A15	1B15
BUF3	1A29	1B29	TADF0	2A14	2B14
BUF4	2A06	2B06	TADF1	2A15	2B15
BUF5	2A07	2B07	TNOOPFN	2A03	2B03
BUF6	2A08	2B08	TNRFCLAN	2A18	2B18
BUF7	2A09	2B09	TRWD	1A24	1B24
BUF8	1A10	1B10	TWNRF	2A04	2B04
CCG	2A19	2B19	TWNRNOPF	1A25	1B25
CREADTPN	2A21	2B21	T7TRCCGN	1A02	1B02

Table 2-6. Cable Connections Between Control Unit and Formatter

CU to Formatter				Formatter to CU			
Signal	PECA Pin Nr	Cable J1 Pin	Cable J1 Earth	Signal	PECA Pin Nr	Cable J1 Pin	Cable J1 Earth
IDEN	5A09	A9	A8	ICCG	5A15	B24	B23
IERASE	6A08	B7	B8	IDBY	6A20	A22	A23
IFEN	5A01	A13	A14	IEOT	6A12	A30	A29
IGO	6A18	A3	A2	IFBY	6A23	B22	B23
ILWD	6A14	B13	B14	IFMK	6A22	A25	A26
IOFL	6A16	A12	A11	IFPT	6A10	A28	A29
IPAR	5A08	B10	B11	IHER	6A21	A24	A23
IREV	5A21	B4	B5	ILDP	5A12	B30	B29
IREW	6A15	B12	B11	IONL	6A09	A27	A26
ITAD0	5A02	A1	A2	IRDY	6A11	B27	B26
ITAD1	5A03	B3	B2	IRP	6A13	A36	A35
IWFM	6A17	B6	B5	IRSTR	6A25	B26	B35
IWRT	5A22	A4	A5	IR0	5A10	B37	B38
IW0	6A07	B16	B17	IR1	5A11	A37	A38
IW1	6A06	A16	A17	IR2	5A13	B39	B38
IW2	6A05	B18	B17	IR3	5A14	A39	A38
IW3	6A04	A18	A17	IR4	5A16	B40	B41
IW4	5A24	B19	B20	IR5	5A17	A40	A41
IW5	5A23	A19	A20	IR6	5A18	B42	B41
IW6	5A25	B21	B20	IR7	5A19	A42	A41
IW7	5A20	A21	A20	IWSTR	6A24	A34	A35
IEDIT	6A19	A6	A5				

2.74 CU Address and Channel Straps

The control unit address code and the channel must be set by wiring straps on card PECB (see Figure 2.17). prior to or during system installation. This control unit must always be strapped for Multiplex Channel working. An example of a strapped address is shown on Figure 2-14 and the logic involved is shown on Figure 2-21, sheet 1 (ADDRESSA and ADDRESSE).

2.75 SPECIAL CIRCUITS

Special circuits are used in the P 831 control unit for clock pulse generation and interfacing with the formatter. Descriptions and diagrams are given in the following paragraphs. The components can be found in the Component Lists (Tables 2-7, 2-8, and 2-9) for this section.

2.76 Clock Pulse Generator

This circuit is a dual one-shot multi-vibrator IC device (Fairchild 9602) mounted on card PECB along with the required discrete components. The circuit diagram is shown in Figure 2-18. A square-waveform output is produced with a pulse width of 3 μ sec.

2.77 Interface Circuits

These circuits provide the interface requirements between the control unit and the formatter. The maximum transmission distance is 6 metres and transmission lines are 120ohm twisted pair cable and 75ohm co-axial cable for the following signals :

CU to formatter				Formatter to CU			
IGO	IREW	IOFL	IFEN	IFMK	IHER	IRSTR	IWSTR

All interface circuits are mounted on card PECA.

2.78 PECOUT Circuits. These circuits provide the matching requirements for control unit output signals to the tape formatter. There are 22 individual PECOUT circuits; four circuits are provided by Fairchild 7438 devices and the remainder by Fairchild 7416 devices. The circuits are shown in Figure 2-19 which includes location, signal, and connector information.

2.79 PECIN Circuits. These circuits provide the matching requirements for input signals to the control unit from the tape formatter. There are 21 individual PECIN circuits which are shown in Figure 2-20 along with location, signal, and connector information.

Table 2-7. Option Components List

Reference	Description	12NC
	PEC A Card	5111 199 85060
	PEC B Card	5111 199 85050
	Strap	5111 199 88410
	Regulator Unit RG4	5111 199 84670
	Rectifier Module RD1	5111 199 86110
	Multicard Rack Equipment Cable	5111 199 83800
	Power Supply Cable	5111 199 83080
	Cable	5111 199 83320

Table 2-8. PEC A Components List

Reference	Description	12NC
	Printed circuit	5111 100 04882
	Connector HE 901 F 62 U	2411 029 11033
	Connector HE 901 F 50 U	2411 029 11032
A4,A5,D4,E3,E5,F1, G4,H3	Integrated circuit 7400	5111 000 00011
A2,B2,D2,F4,F5,G2, G3	Integrated circuit 7402	5111 000 00031
B3,B6,C6,F6,G1,H2, H6	Integrated circuit 7404	5111 000 00051
E2	Integrated circuit 7410	5111 000 00081
D6,E6,G6	Integrated circuit 7416	5111 000 00101
F2	Integrated circuit 7450	5111 000 00171
F3	Integrated circuit 7453	5111 000 00181
A6	Integrated circuit 7438	5111 000 00151
B4,B5,C5,D5,E4,H4,A1	Integrated circuit 7474	5111 000 00221
D1,E1	Integrated circuit 7475	5111 000 00231
A2	Integrated circuit 74193	5111 000 00351
C3,C4	Integrated circuit 9309	5111 000 00511
C2,D3	Integrated circuit 9314	5111 000 00531
B1,C1,H1	Integrated circuit 9322	5111 000 00551
C1,C2	Capacitor FITCO 10µF 25V	2222 015 16109
C3-C48	Capacitor PMA 10000pF ± 20%, 250V	2011 301 52252
R1-R6	Resistor 1KΩ, ± 1% , 0.125W	5122 000 01041
R7-R27	Resistor 215Ω, ± 1% , 0.125W	5122 000 00881
R28-R48	Resistor 316Ω, ± 1% , 0.125W	5122 000 00921
	Shorting Link CV 213	2411 024 01007

Table 2-9. PEC B Components List

Reference	Description	12NC
	Printed Circuit	5111 100 04891
	Connector 00 6041 062 000 003	2422 022 98012
B2,B3,B4,D3,D5,F7,H7	Integrated circuit 7400	5111 000 00011
A3,B7,C4,E4,E7,G5	Integrated circuit 7402	5111 000 00031
E1,F1,G1,H1	Integrated circuit 7403	5111 000 00041
A1,C3,D4,F4,G6	Integrated circuit 7404	5111 000 00051
A2,H3,D6,H5	Integrated circuit 7410	5111 000 00081
C5,E5,F6	Integrated circuit 7420	5111 000 00121
C7	Integrated circuit 7437	5111 000 00141
G7	Integrated circuit 7438	5111 000 00151
G3,H7	Integrated circuit 7450	5111 000 00171
B6,F3,G4,H4	Integrated circuit 7473	5111 000 00211
A4,A5,B5,C6,F5	Integrated circuit 7474	5111 000 00221
E3,H6	Integrated circuit 7476	5111 000 00241
D2	Integrated circuit 9301	5111 000 00501
E2,F2,G2,H2	Integrated circuit 9322	5111 000 00551
A6,A7,E6	Integrated circuit 7430	5111 000 00131
C8	Integrated circuit 9602	5111 000 00571
C1,C2	Capacitor FITCO 10µF, 25V	2222 015 16109
C3-C42	Capacitor ceramic tube 10000pF, 500V	2222 552 03103
C43-C44	Micro Capacitor 330pF, ± 1% , 125V	2222 425 43301
R1-R8	Resistor 6.19KΩ, ± 1% , 0.125W	5122 000 01231
R9-R16	Resistor 3.16KΩ, ± 1% , 0.125W	5122 000 01161

Reference	Description	12NC
R17-R20	Resistor 1KΩ, 1%, 0.125W	5122 000 01041
R21-R22	Resistor 23.7KΩ, 1%, 0.125W	5122 000 01371
B1	Integrated circuit 9324	5111 000 00561

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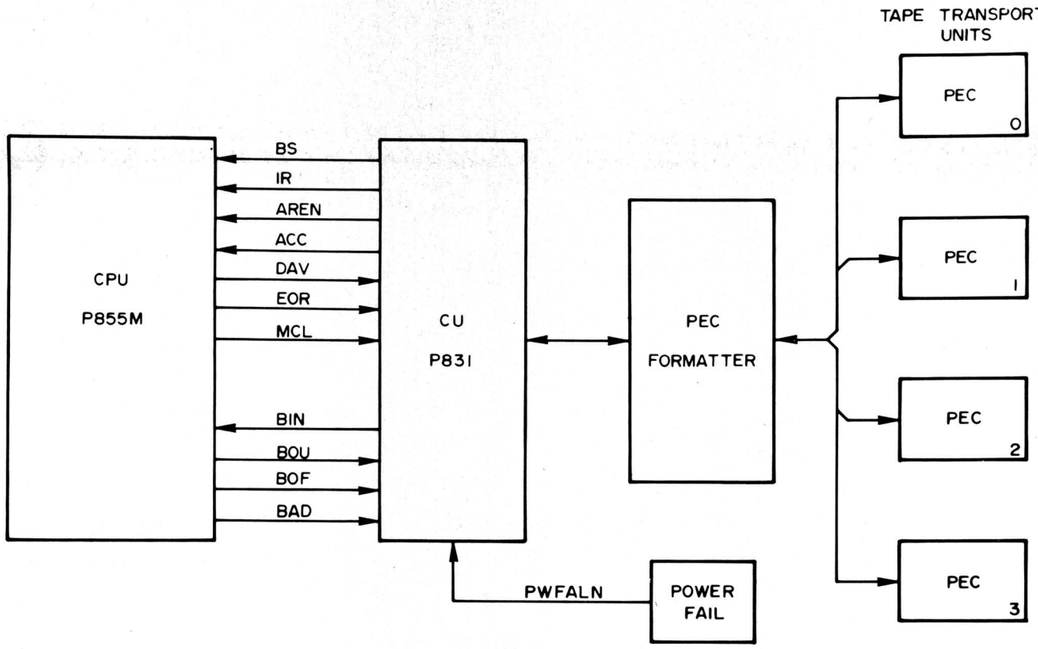

Figure 2-1. P855M Magnetic Tape Subsystem Block Diagram

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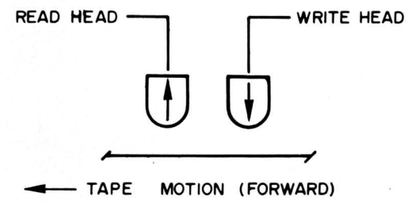
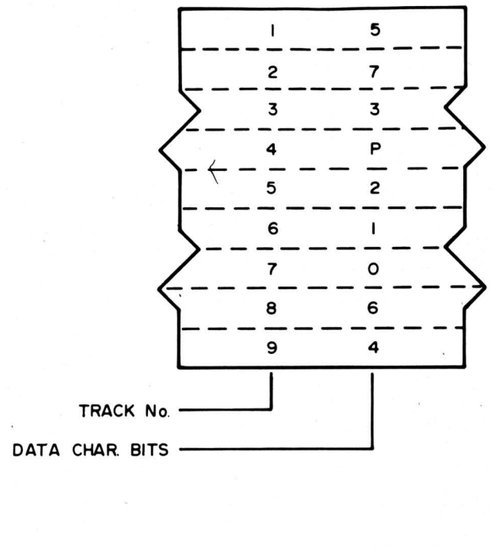




Track Number	Binary Value	EBCDIC Bits	ASCII 8 Bits	File Mark Code
4	P	P	8	0
7	2^7	0	0	0
6	2^6	1	1	0
5	2^5	2	2	0
3	2^4	3	3	1
9	2^3	4	4	0
1	2^2	5	5	0
8	2^1	6	6	1
2	2^0	7	7	1

Figure 2-2. Track Format

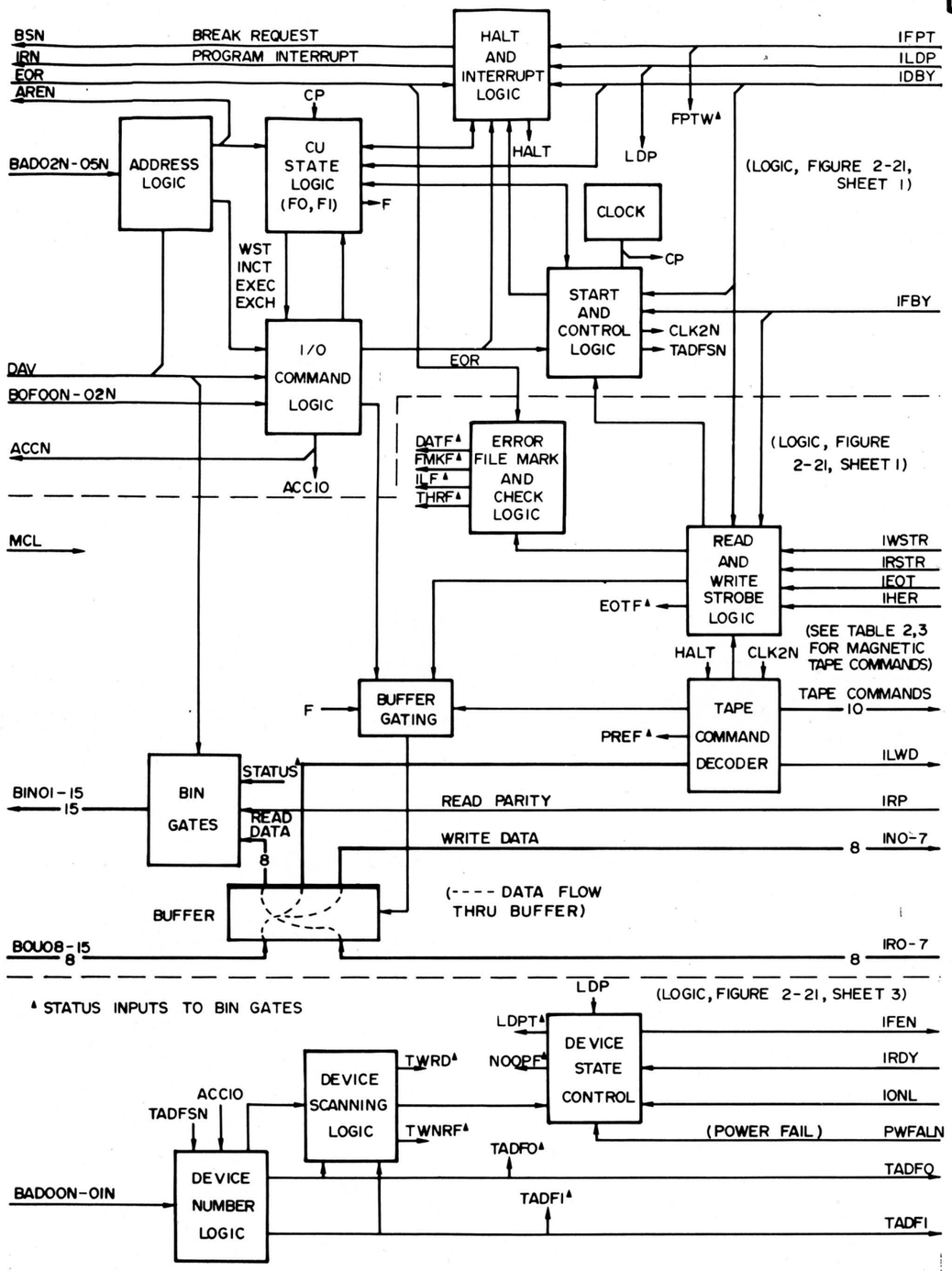
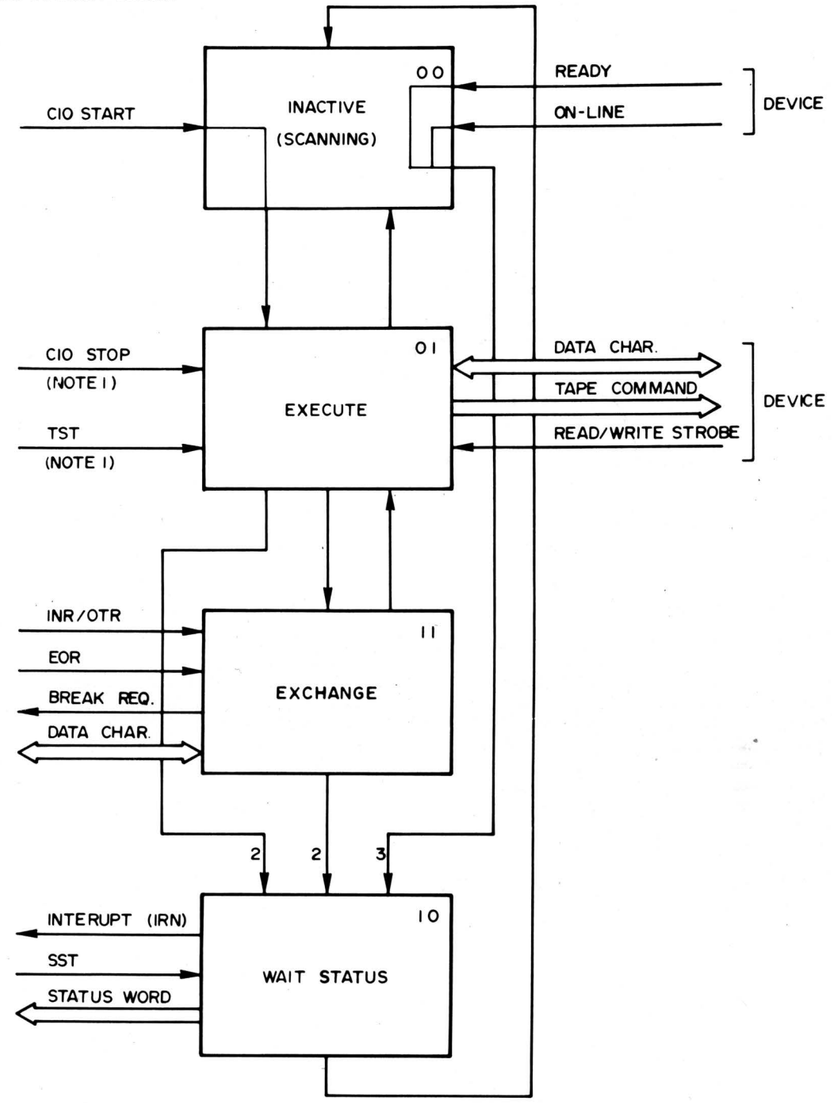


Figure 2-3. P831 Magnetic Tape CU Simplified Block Diagram

THE OPERATIONAL STATE CODE (F0, F1) IS SHOWN IN EACH BLOCK.



NOTES: 1 THESE SIGNALS MAY BE RECEIVED IN ANY OPERATIONAL STATE

2 END OF EXCHANGE (EOT, EOR) OR FAULT CONDITION

3 AFTER ACCEPTING A REWIND OR OFF LINE COMMAND

Figure 2-4. Operational States

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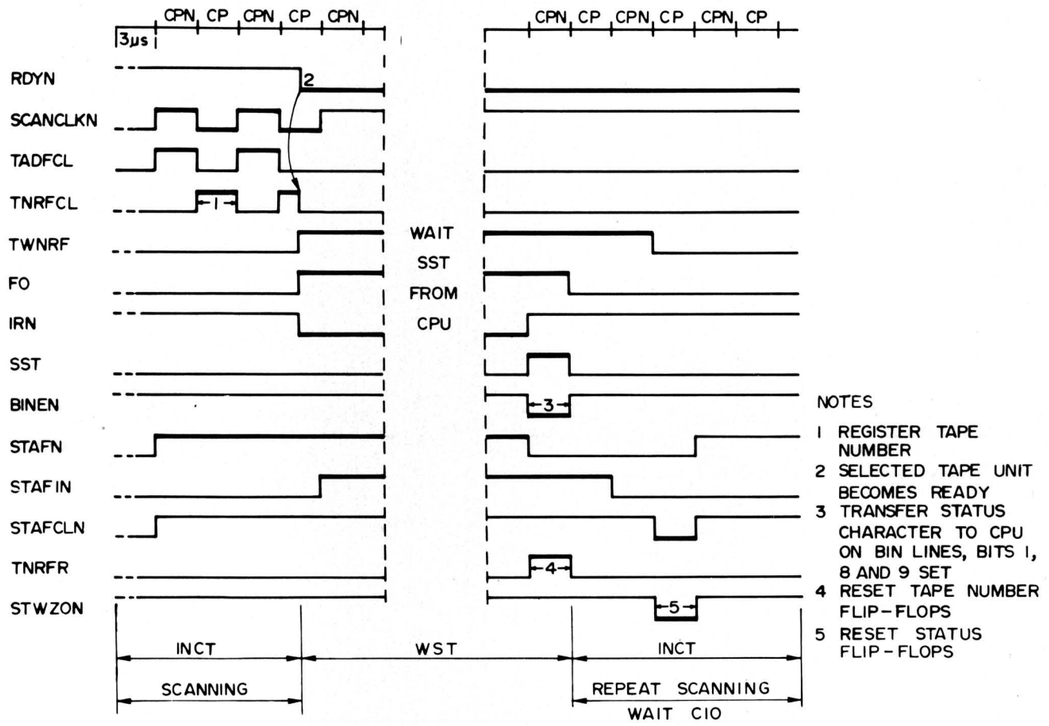

Figure 2-5. Scan Timing

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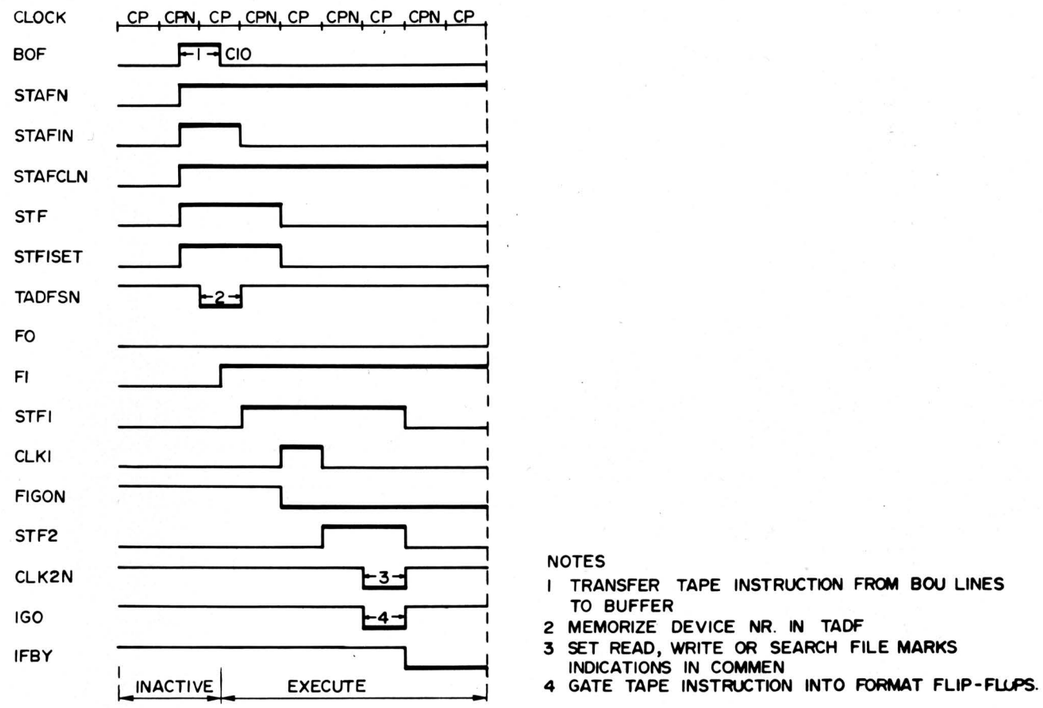


Figure 2-6. Tape Instruction Initial Timing

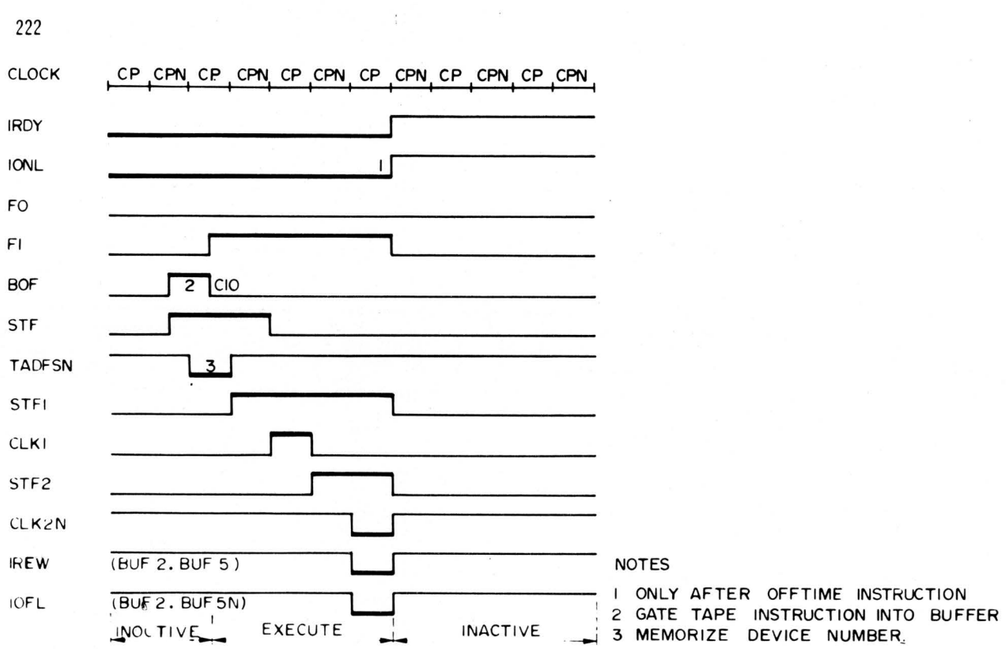
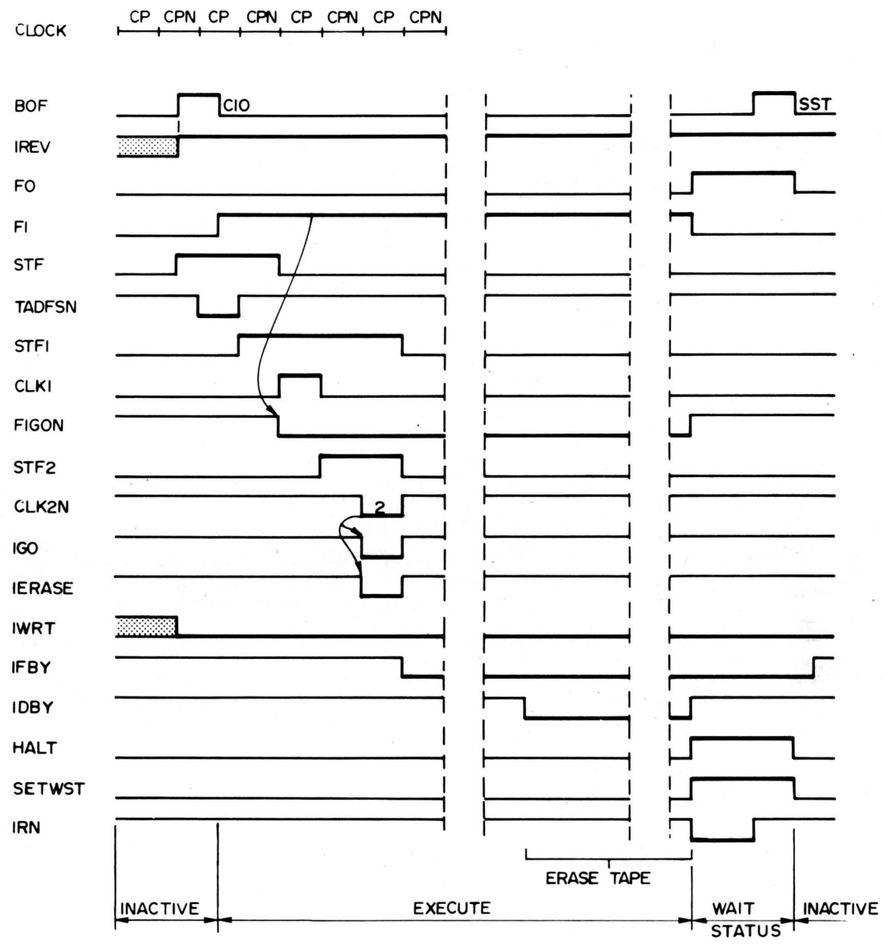
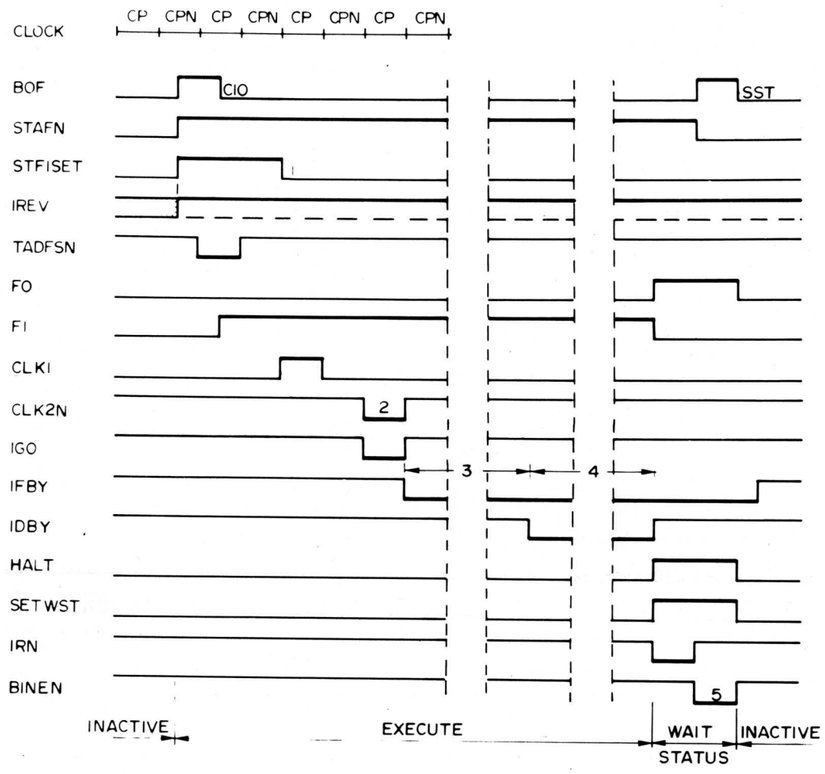


Figure 2-7. Off Line and Rewind Timing



NOTES
1 HIGH FOR FORWARD, LOW FOR BACKWARD.
2 INITIATE FORMATTER.

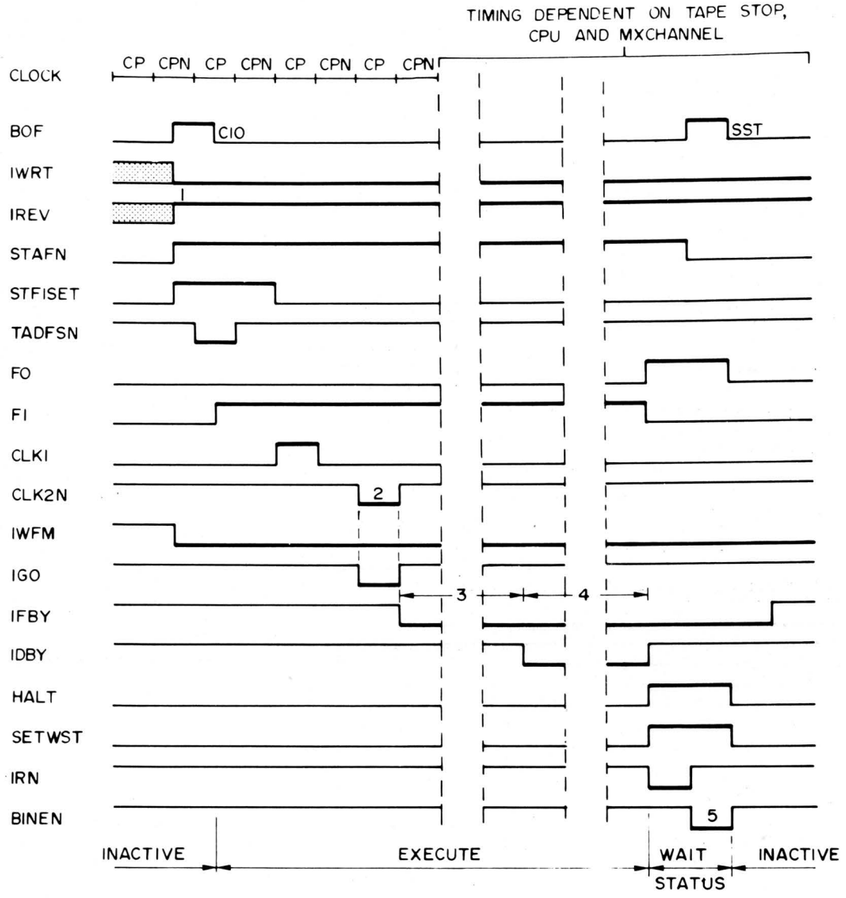
Figure 2-8. Erase Gap Timing



NOTES

1 HIGH FOR FORWARD, LOW FOR BACKWARD.
2 INITIATE FORMATTER.
3 WAIT UNTIL DEVICE GETS UP TO SPEED.
4 EXECUTE OPERATION ON DEVICE.
5 TRANSFER STATUS WORD TO CPU.

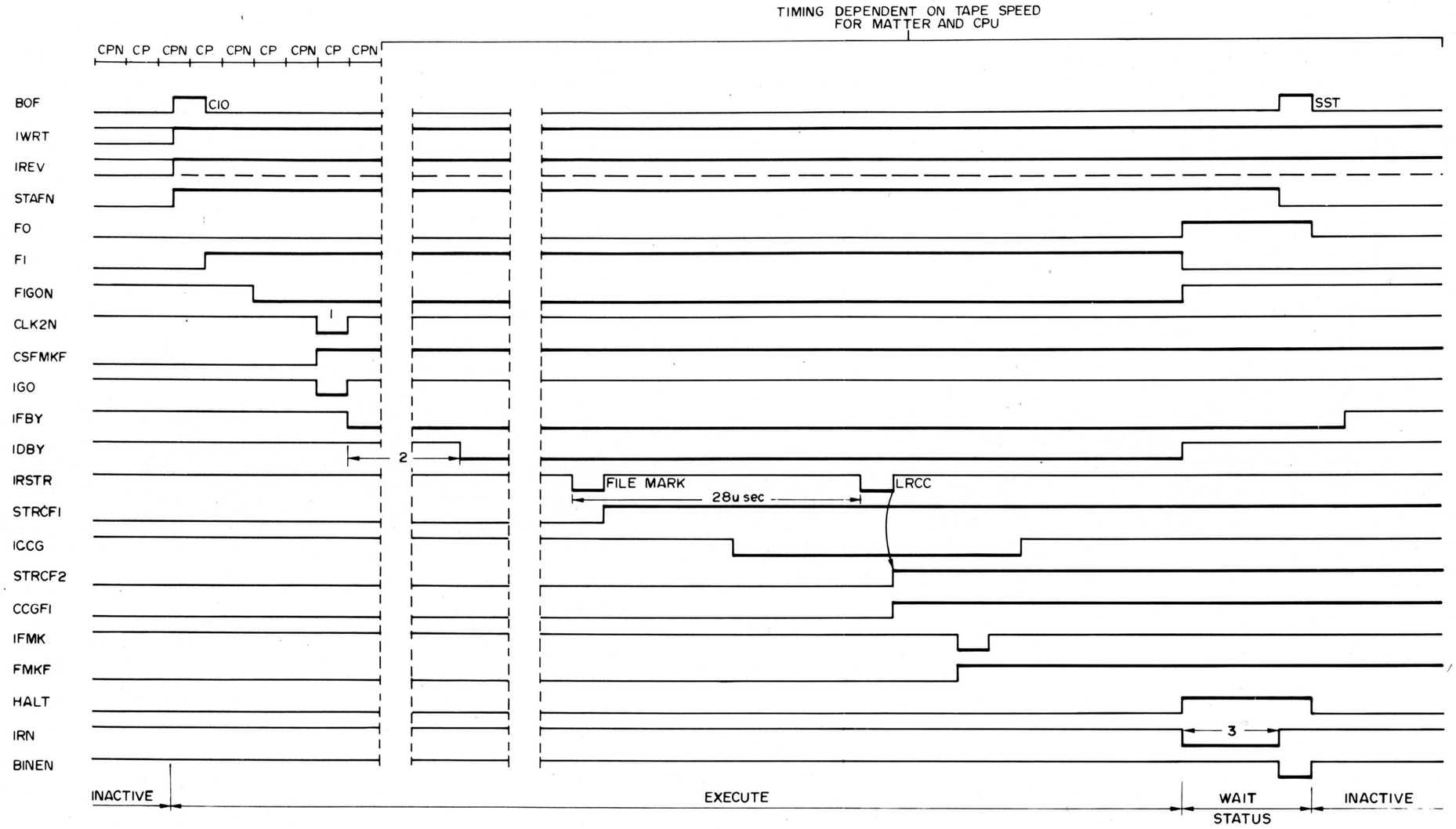
Figure 2-9. Space One Block (Forward/Backward)



NOTES

1 HIGH FOR FORWARD, LOW FOR BACKWARD.
2 INITIATE FORMATTER.
3 DELAY UNTIL DEVICE GETS UP TO SPEED AND FOR FILE MARK GAP.
4 EXECUTE OPERATION ON DEVICE.
5 TRANSFER STATUS WORD TO CPU.

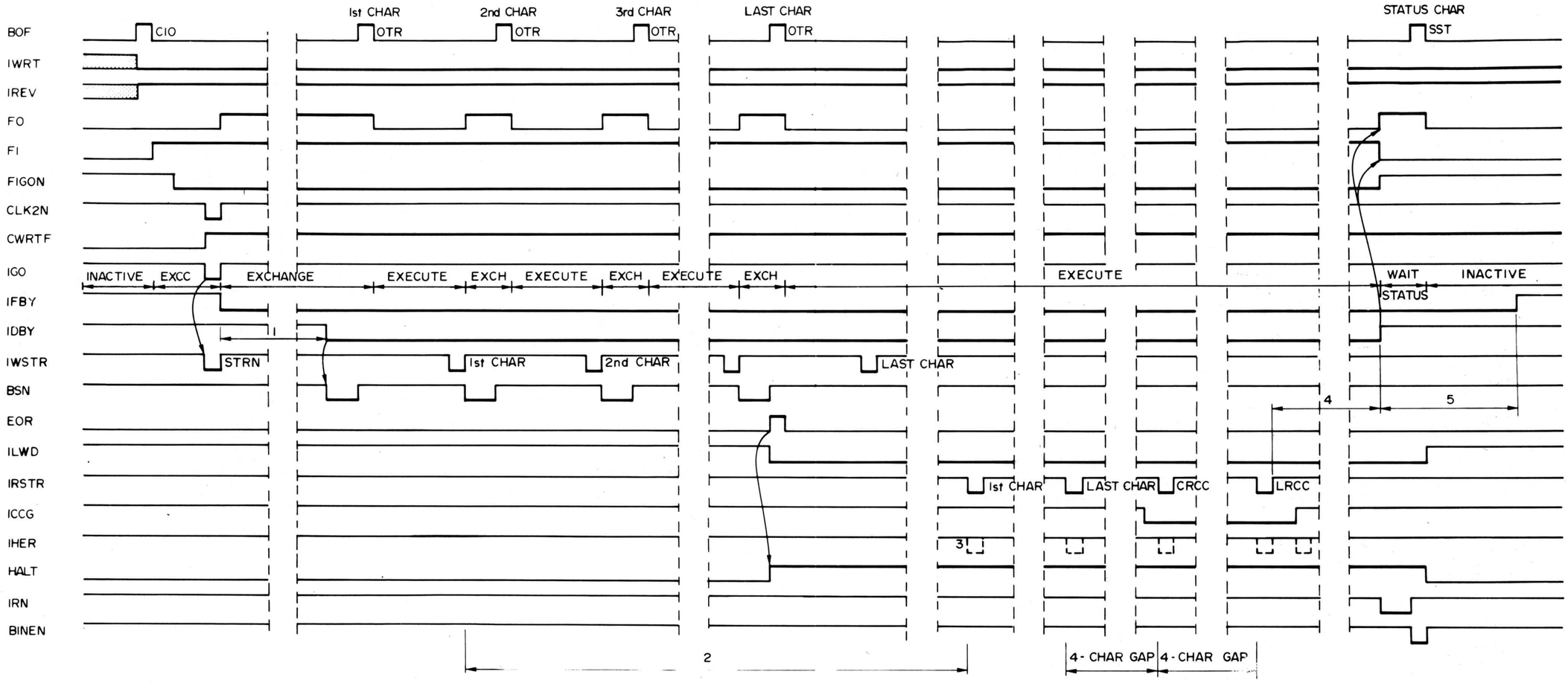
Figure 2-10. Write, File Mark



NOTES

1 INITIATE FORMATTER
2 DELAY UNTIL DEVICE GETS UP TO SPEED
3 TIMING DEPENDENT ON CPU

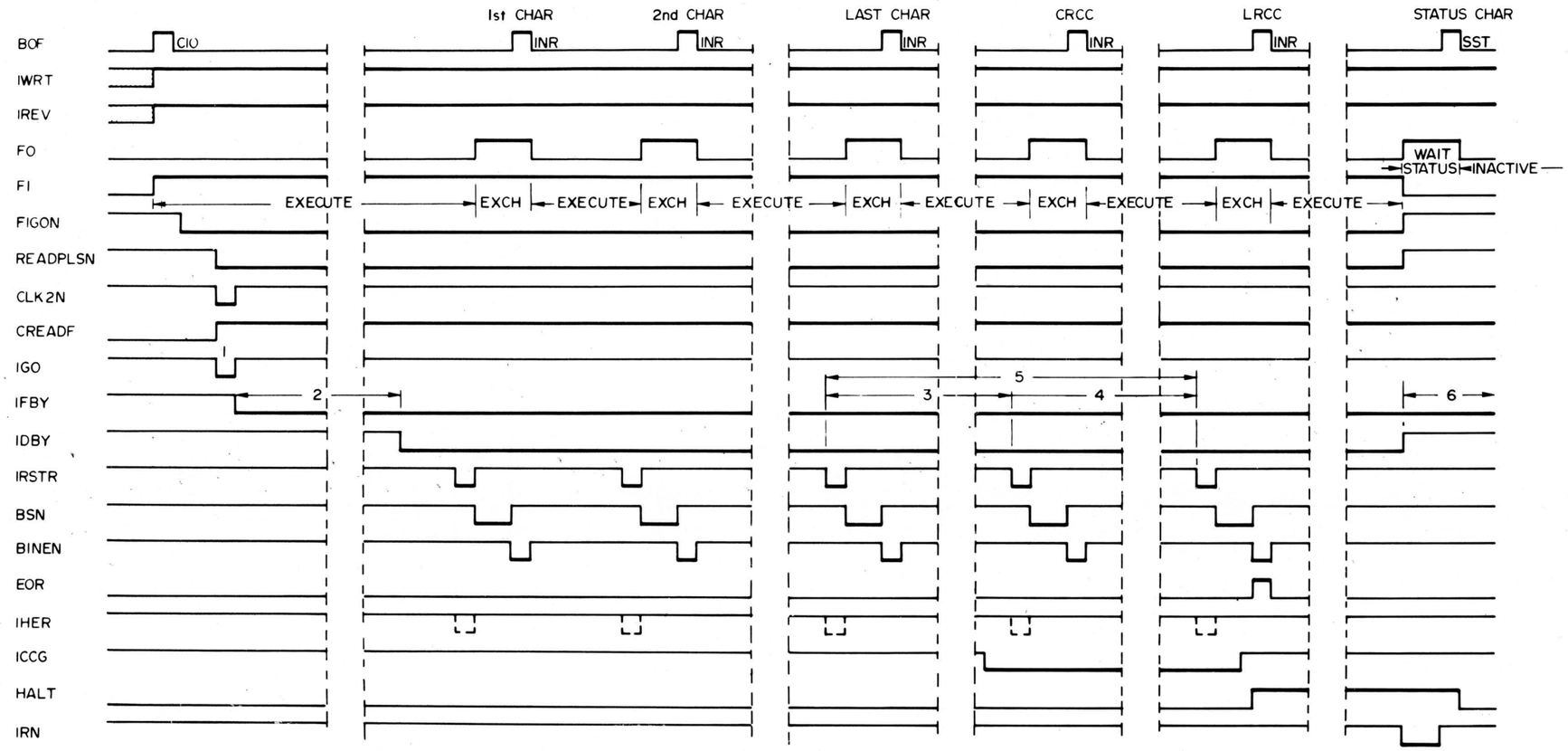
Figure 2-11. Search File Mark (Forward/Backward)



NOTES

1. PRE-RECORD DELAY (ALLOWS DEVICE TO GET UP TO SPEED)
2. HEAD GAP DELAY (TIME BETWEEN WRITING FIRST CHAR AND READING IT)
3. THE HARD ERROR INDICATION OCCURS, IF THERE IS A DATA FAULT
4. POST-RECORD DELAY
5. RAMP-DOWN DELAY

Figure 2-12. Write One Block



NOTES

1 INITIATE FORMATTER
2 PRE-RECORD DELAY (ALLOWS DEVICE TO GET UP TO SPEED)
3 FOUR CHAR. GAP FOR LRCC
4 FOUR CHAR GAP FOR CRCC
5 WITH 7-TRACK TRANSPORT THERE IS NO CRCC
6 IFBY GOES INACTIVE AT THE END OF THE RAMPDOWN DELAY

Figure 2-13. Read One Block

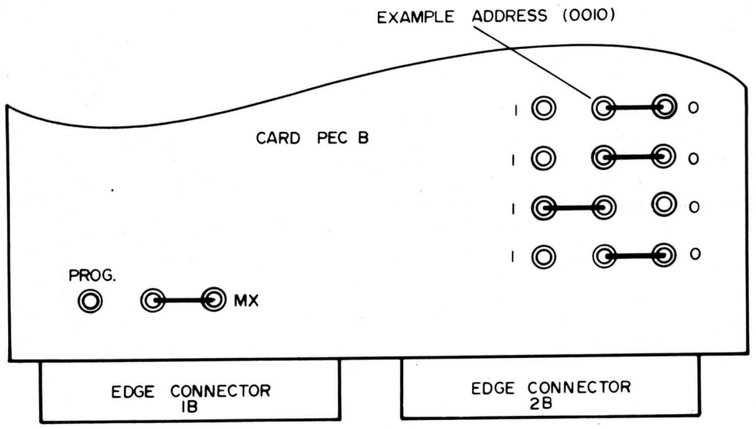
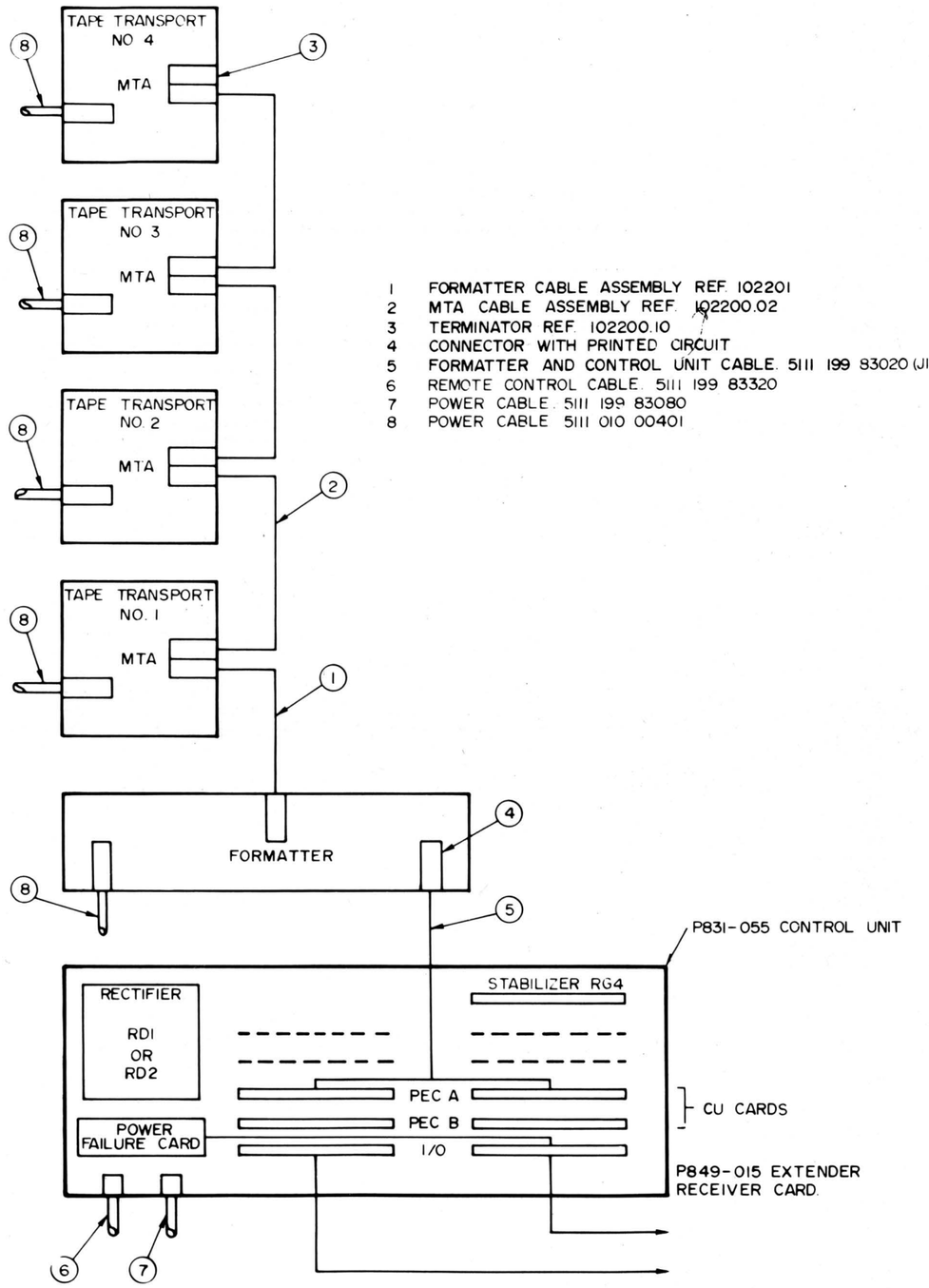


Figure 2-14. Control Unit Address and Channel Straps



1 FORMATTER CABLE ASSEMBLY REF. 102201
2 MTA CABLE ASSEMBLY REF. 102200.02
3 TERMINATOR REF. 102200.10
4 CONNECTOR WITH PRINTED CIRCUIT
5 FORMATTER AND CONTROL UNIT CABLE. 5111 199 83020 (J1)
6 REMOTE CONTROL CABLE. 5111 199 83320
7 POWER CABLE. 5111 199 83080
8 POWER CABLE 5111 010 00401

Figure 2-15. Magnetic Tape System Layout

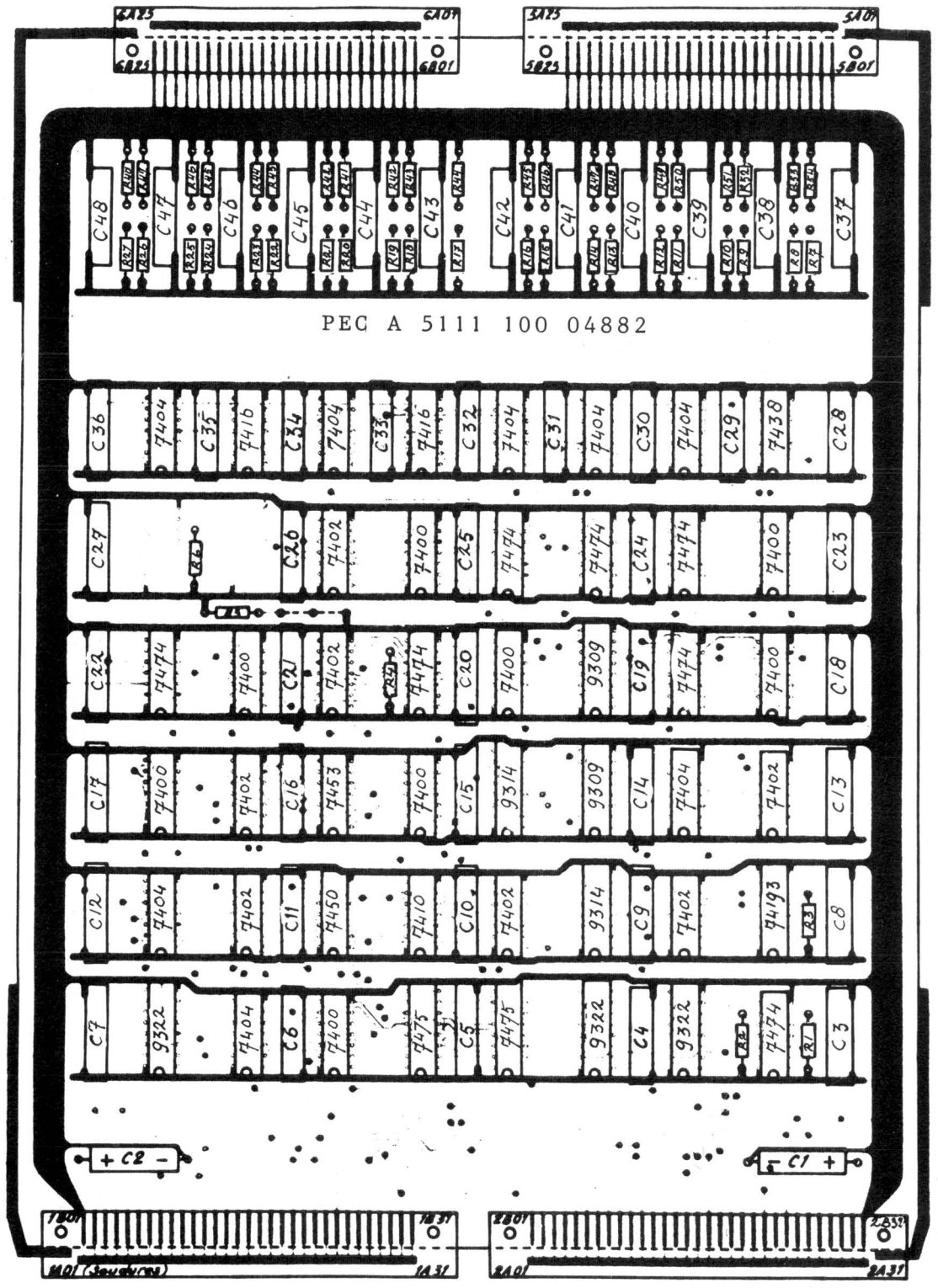


Figure 2-16. Card PECA Layout

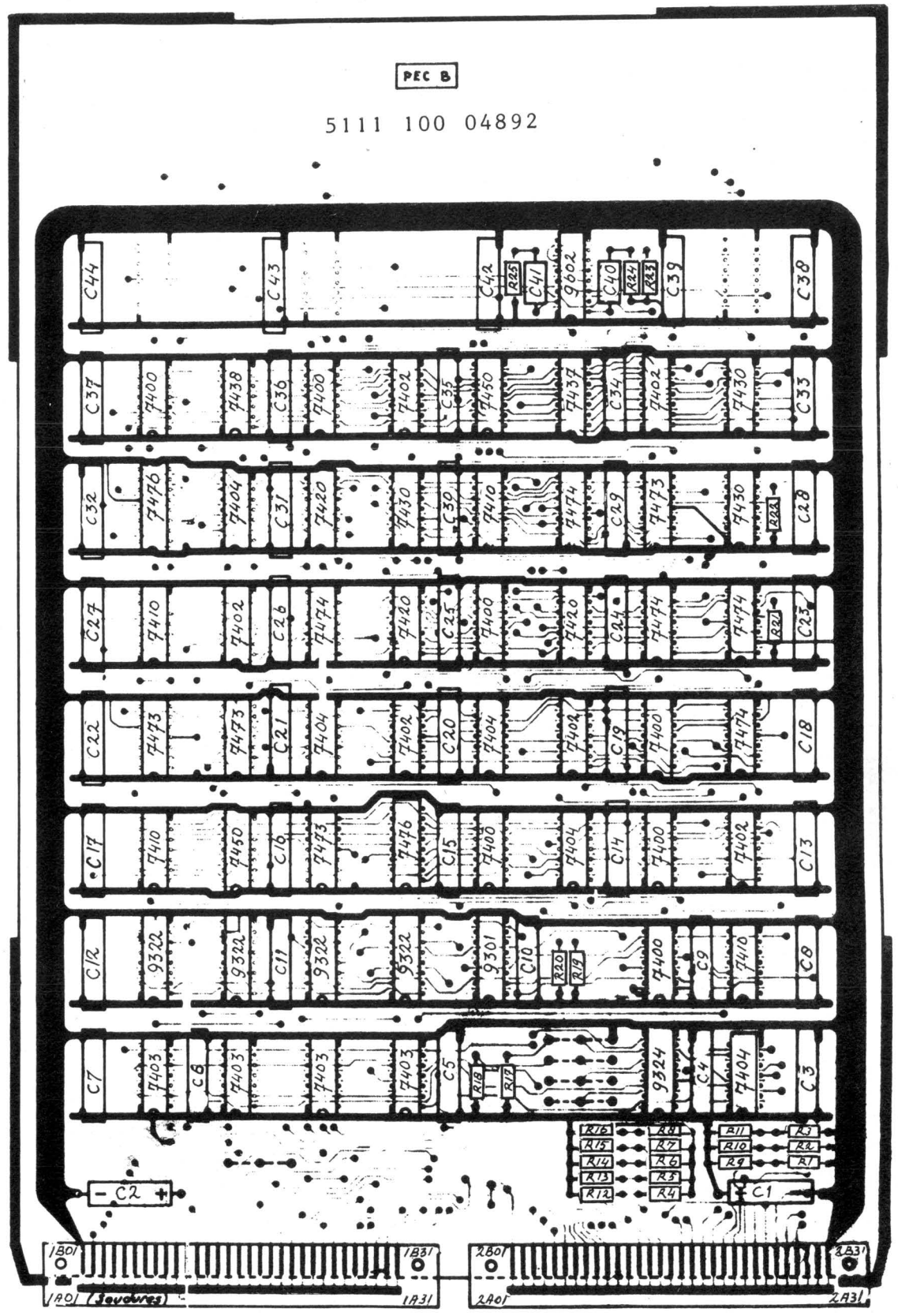


Figure 2-17. Card PECB Layout

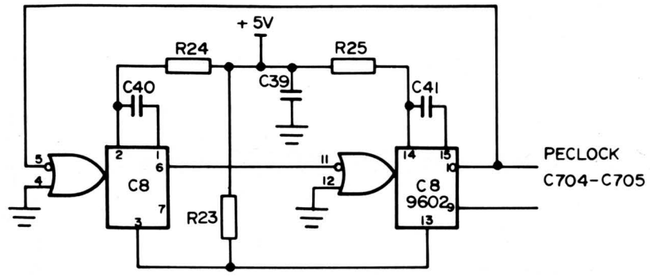
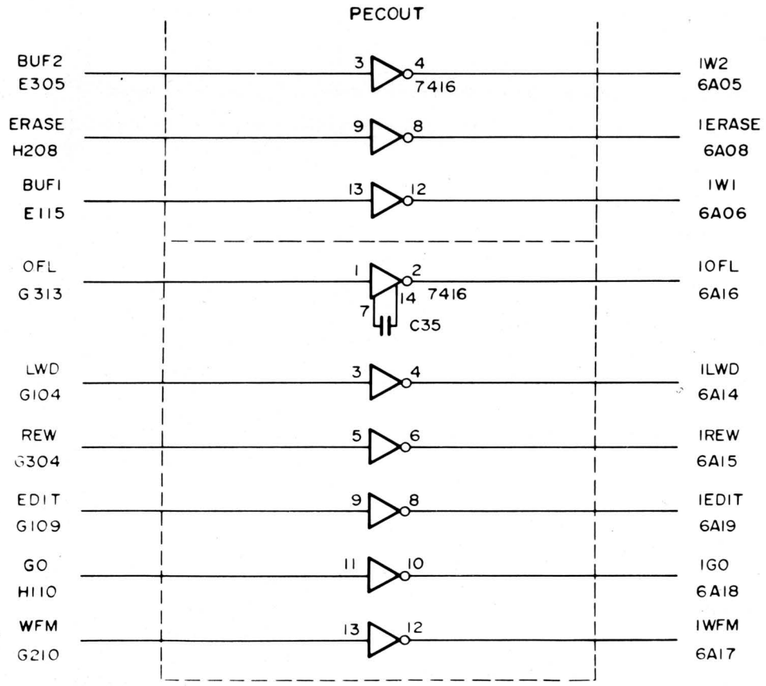


Figure 2-18. Clock Pulse Generator Circuit



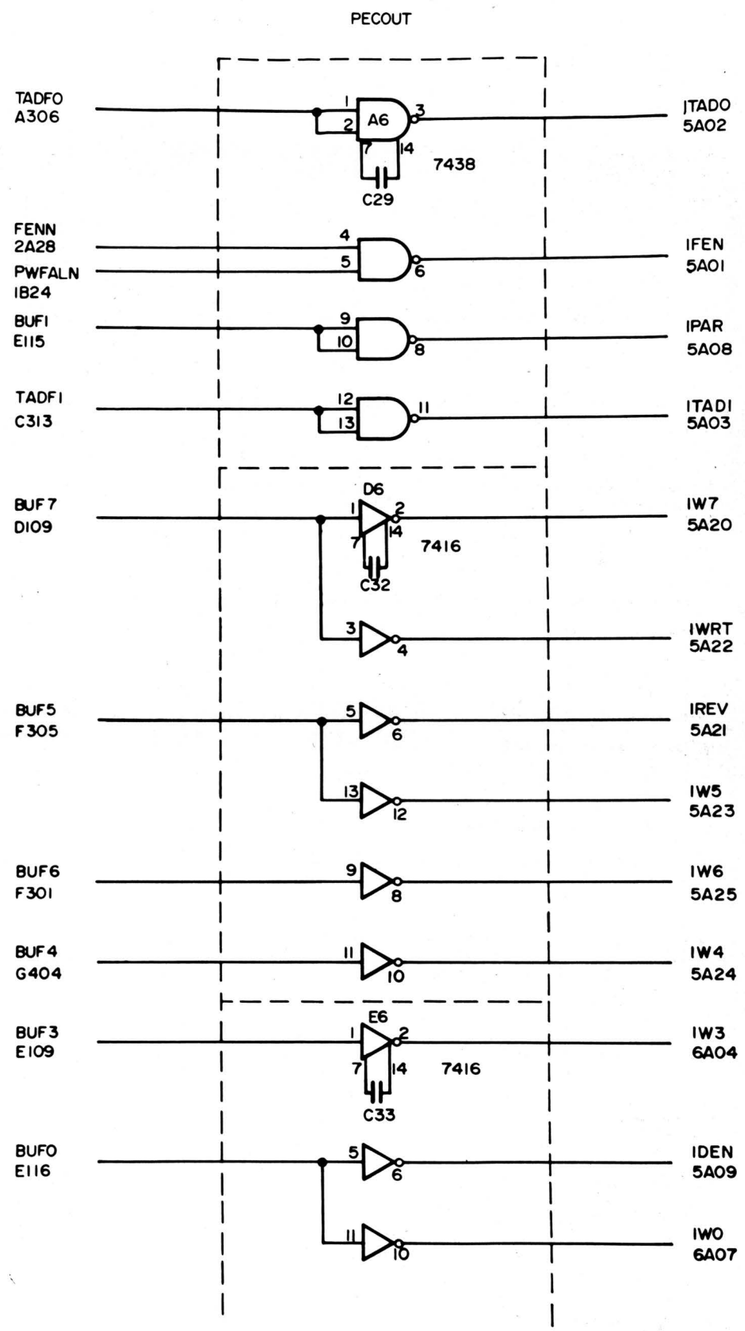


Figure 2-19. PECOUT Interface Circuits

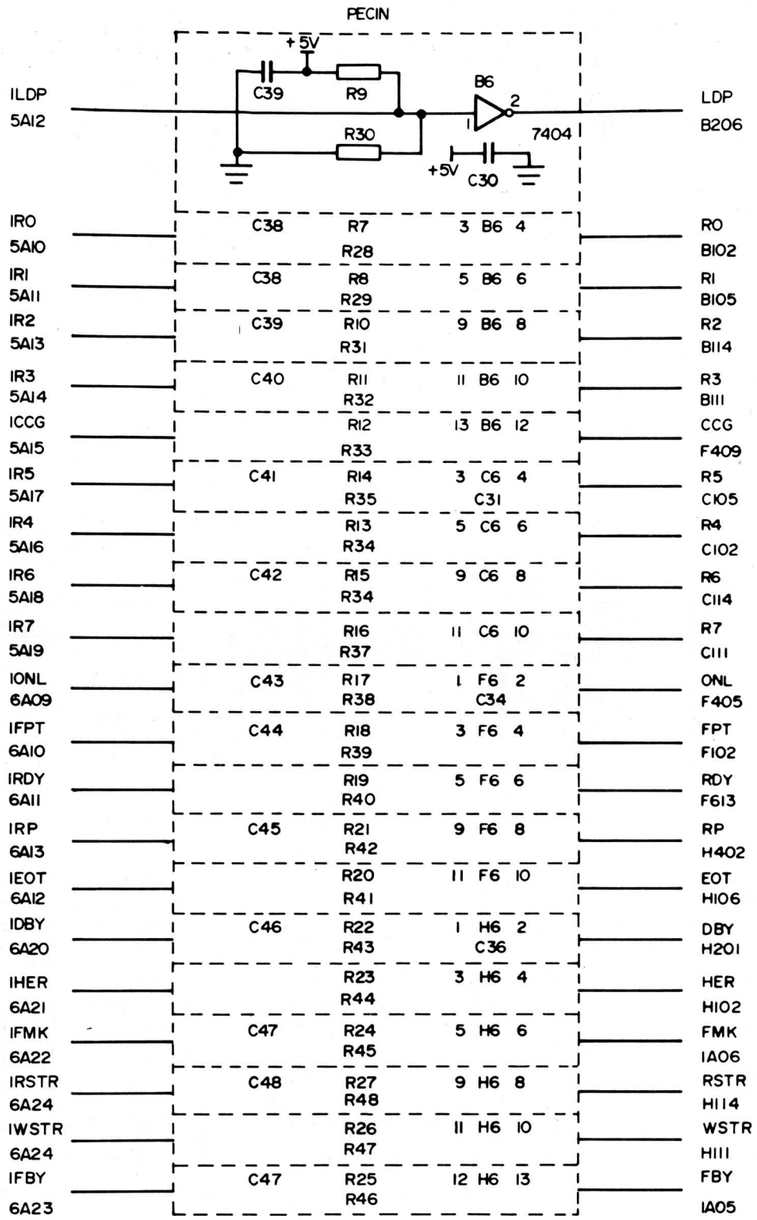


Figure 2-20. PECIN Interface Circuits

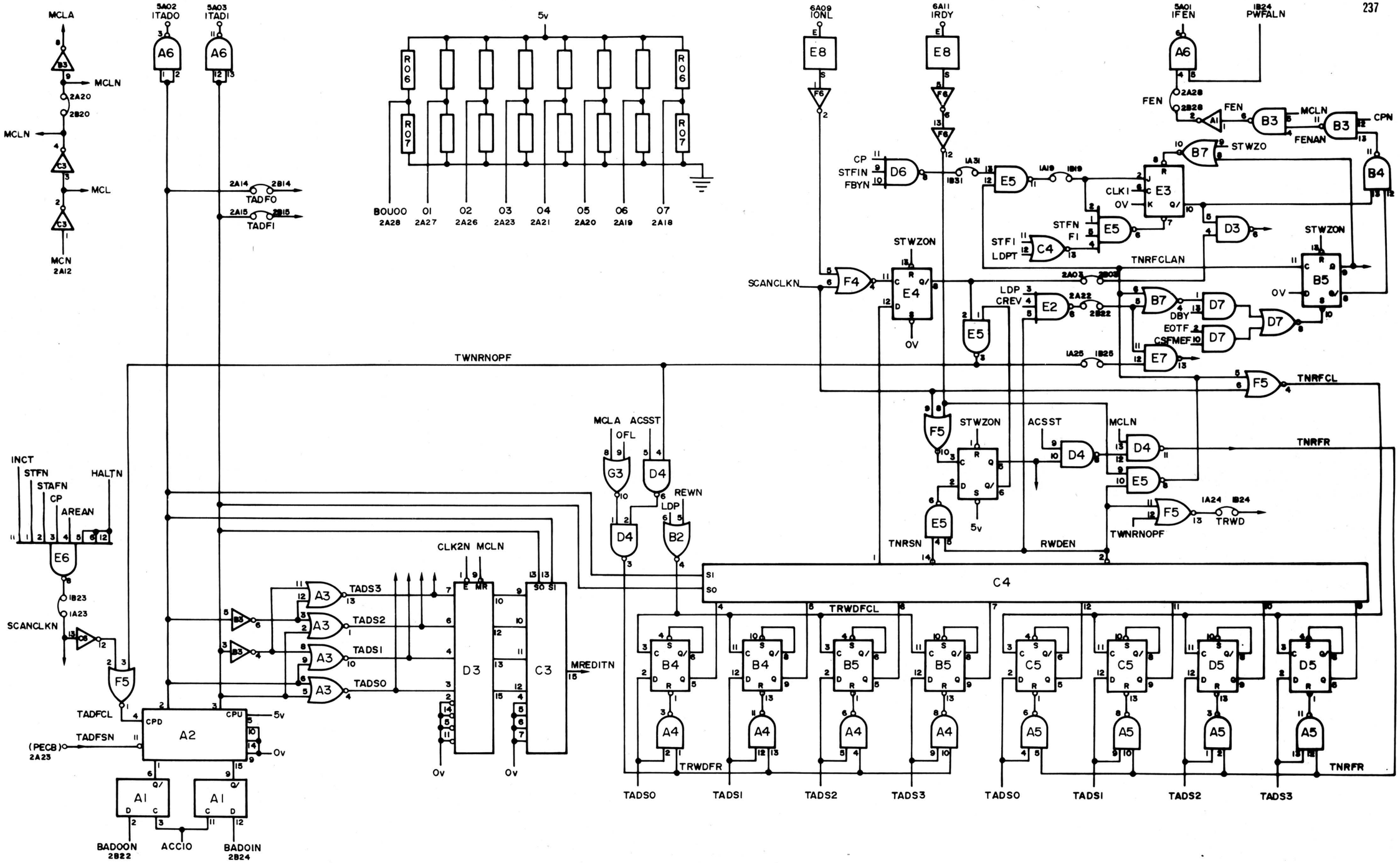


Figure 2-21. LOGIC 1 (Sheet 1 of 3)

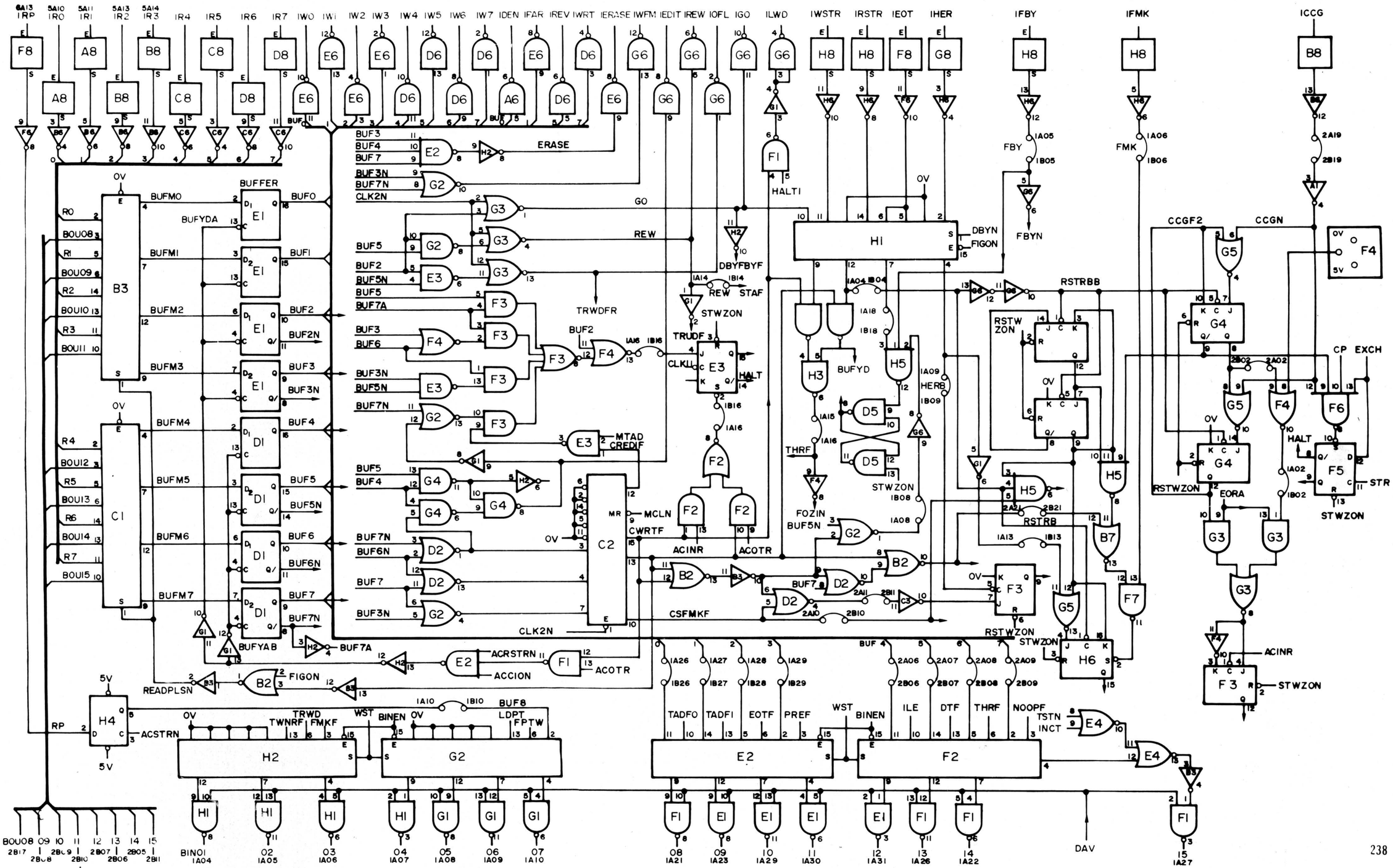


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Figure 2-21. LOGIC 2 (Sheet 2 of 3)

STATE	FI	FO
INCT	0	0
EXCH	1	1
EXEC	0	1
WST	1	0

Figure 2-21. LOGIC 3 (Sheet 3 of 3)